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Fuzzy logic controller based DC-Link Voltage Self-Balance Method for Multilevel Converter with less Number of Voltage Sensors

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Abstract—In many inverters, Voltage balance of dc-link capacitors is very important for applications of a cascade multilevel converter or a modular multilevel converter. In this paper, a novel diode-clamped modular multilevel converter (DCM^2 C) topology is proposed and a power feedback control method is developed with fuzzy logic controller. With the developed control strategy, the proposed diode-clamped circuit becomes controllable closed loop which enables the capacitor voltages to be clamped by low power rating clamping diodes. The proposed topology and control strategy has quicker response with transient state error reduction and requires much fewer voltage sensors than the normally used traditional method of multilevel inverters as diode clamped inverters; therefore, the system performance improvement and cost reduction are expected. Based on the proposed DCM^2 C, a novel N +1-level cascade multilevel topology is proposed for a cascade active power filter (CS-APF). The Proposed fuzzy logic controller is implemented to get study state response at dc voltage capacitors, therefore to get balanced load outputs. The simulation results from the CS-APF have demonstrated and verified the effectiveness of the proposed novel topology and control method.

Index Terms—Capacitor voltage balance, cascade active power filter (CS-APF), diode-clamped modular multilevel converter (DCM^2 C), minimum number of voltage sensors, fuzzy logic controller.

I. INTRODUCTION

Now a day's power converters are playing key role in power system applications. Power electronic devices with less losses and useful for medium and high power applications causes to grow, for instance, an active power filter (APF) which is an ideal choice for power conditioning [1]–[3]. A high switching frequency is normally required for such electronic converters to achieve good performance, such as fast response, good filtering, and low harmonics; however, the high switching frequency may limit the capacity of a normal two-level converter due to the power loss.

A multiple converter configuration may be an effective solution for high-power medium-voltage applications [4]–[7], but a bulky transformer is usually required. Recently, the topologies of multilevel converter have become popular in medium-voltage applications, because of its features of simple structure, modularity, and transformer-less. In particular, the multi modular converter based on half-bridge or full-bridge topology is a good solution for medium-/high-voltage applications, including STATCOM, APF, and HVDC. However, the dc-link capacitors are floating in either a full-bridge cascade converter or a half-bridge cascade converter. Due to the difference of parasitic parameters between cells, the non ideal drive pulses, and so on, the dc-link capacitor voltages may become unbalanced if a specifically de-signed control method is not in place. Some capacitor voltage balance control algorithms are studied. These methods may be classified into the following categories:

1) Switching patterns rotated (SPR) methods;

2) Fundamental voltage vector regulation (FVVR) methods; and

3) Direct duty cycle (DDC) control methods.

By adding an auxiliary circuit to each cell for exchanging energy between cells, capacitor voltage balance can also be realized. However, such an auxiliary circuit usually requires an extra inverter and a control circuit, maybe also a transformer if isolation

is required, which will significantly Increase the circuit complexity and cost.

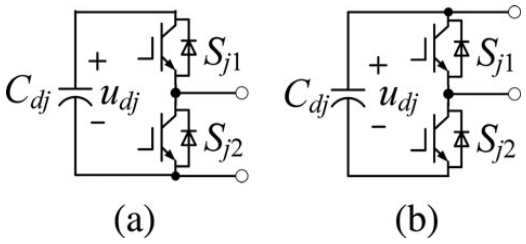

Fig.1.Two basic topologies of a half-bridge cell.

A novel simple diode-clamped modular multilevel converter (DCM^{2}C) topology is proposed in this paper. It is based on the cascade connection of half-bridge cell converters. Via adding a clamping diode to each cell's dc bus, the capacitor's voltage of one cell could be clamped by the two neighboring cells when the circuit works. At the same time, an energy feedback cir-cuit is used for connecting the top and bottom cells, so that a closed loop clamping circuit is formed. In this topology, only the top and bottom cells need the voltage sensors, which significantly reduce the required number of sensors. Furthermore, a performance enhancing control algorithm is implemented in the controller to ensure a quick response.

The proposed novel topology may be used in any converter with half-bridge cascade topology. A novel three-phase DCM^2 C topology with star configuration which can be used for VAR com-sensation or harmonics suppression is presented for discussion in this paper. There are 3(N−1) diode-clamped cells and one common cell in the topology. A total of four dc-link voltage sensors are needed for the three top cells and the common cell. The control of the three-phase DCM^2 C applied as a CS-APF is discussed in this paper. The effectiveness of the novel topology and control method is validated by simulation.

II. TOPOLOGY AND PRINCIPLES OF A DCM^2 C

A. Topology of a DCM^2 C

The two basic topologies of a half-bridge converter cell are shown in Fig. 1, where the dc-link capacitor is completely floating.

The two proposed DCM^2 C topologies (cell topology) are shown in Fig. 2(a) and (b). Each topology is a two-port network. In Fig. 2(a), the cathode of the clamping diode D_j is connected to the positive polarity of the capacitor, while the diode's anode is connected to the capacitor's negative polarity in Fig. 2(b). x and x' are the terminals for connecting the neighboring cells on dc side, while y and y' are the terminals on ac side.

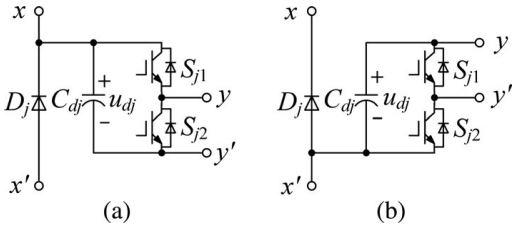

Fig.2. Topologies of the proposed diode-clamped half-bridge cell.

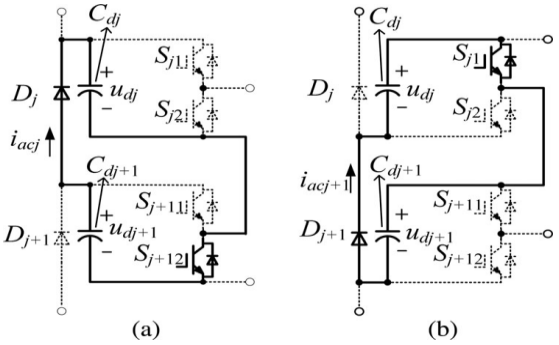

Fig.3. Voltage-clamped switch mode of the two topologies

Fig. 3(a) shows an upward clamping topology (UCT) of a DCM^2 C. If $u_{dj} < u_{dj+1}$ (u_{dj} is the voltage of the capacitor C_{dj} and u_{dj+1} is the voltage of C_{dj+1}), there will be a current i_{acj} flowing through D_j when the switch S_{j+12} is ON (neglecting the voltage drop of the diode and the saturation voltage of the switch), as shown in Fig. 3(a). Then, u_{dj} will rise and u_{dj+1} will drop until $u_{dj} = u_{dj+1}$. If $u_{dj} \geq u_{dj+1}$, the diode D_j will keep OFF. Thus, the capacitor voltage relationship is $u_{d1} \geq u_{d2} \geq u_{dN}$. _>u_{d1} is the dc voltage of the top cell, and u_{dN} is the dc voltage of the bottom cell.

Consequently, if u_{d1} could be clamped at the same level as u_{dN} , all capacitors would have the same voltage. Fig. 3(b) shows a downward clamping topology (DCT), which uses the similar principle to

the UCT's. If $u_{dj+1} < u_{dj}$, C_{dj+1} will be clamped by C_{dj} when S_{j1} is ON, as shown in Fig. 3(b).

Now, the key point is to realize $u_{d1} = u_{dN}$. The following part presents a method to solve the problem by using an energy feedback circuit to form a closed voltage clamping loop with the clamping diodes. Several energy feedback topologies are proposed.

Fig. 4(a) shows an energy feedback topology based on an auxiliary full-bridge inverter (AFBI) which shares the dc bus with the top cell of the UCT (or with the bottom cell of the DCT). The ac side of the AFBI is connected to the primary of an isolation transformer T_{ac} . The secondary of T_{ac} is connected with a rectifier that shares the dc bus with the bottom cell of the UCT (or with the top cell of the DCT). The winding turning ratio of T_{ac} is 1: w_T .

When the AFBI works as a square wave ac inverter (The output voltage of the inverter is u_{ac} .), a square wave voltage with the same amplitude as u_{ac} ($w_T = 1$) will be induced at the secondary side of T_{ac} . The induced ac voltage is converted into a dc voltage by the rectifier. If the dc voltage of cell N is lower than that of cell 1, energy will be transmitted from C_{d1} to C_{dN} via the feedback circuit. Then, u_{dN} will rise and u_{d1} will drop, so u_{d1} and u_{dN} will be equalized by the feedback circuit. Therefore, a closed voltage clamping circuit is realized.

Considering the leakage inductance of T_{ac} and the voltage drop of the switches, w_T should be a little larger than 1, and the output power of the auxiliary circuit can be controlled by adjusting the pulse width modulation (PWM) duty cycle of cell 1.

The AFBI needs four active switches, while an auxiliary half bridge inverter (AHBI) needs only two active switches as shown in Fig. 4(b), and the winding turning ratio of the transformer is 1: wT = 1: 2 (Similarly, wT > 2 in practical application). Besides, a capacitor Cac is connected to the primary winding of Tac in series to block the dc component. DC-link voltage unbalance is mainly caused by the loss difference between cells and the non ideal drive pulses, and such unbalance could be removed with much lower power comparing with that of the main circuit. Then, another feedback topology with a simpler structure is proposed, as shown in Fig. 4(c).

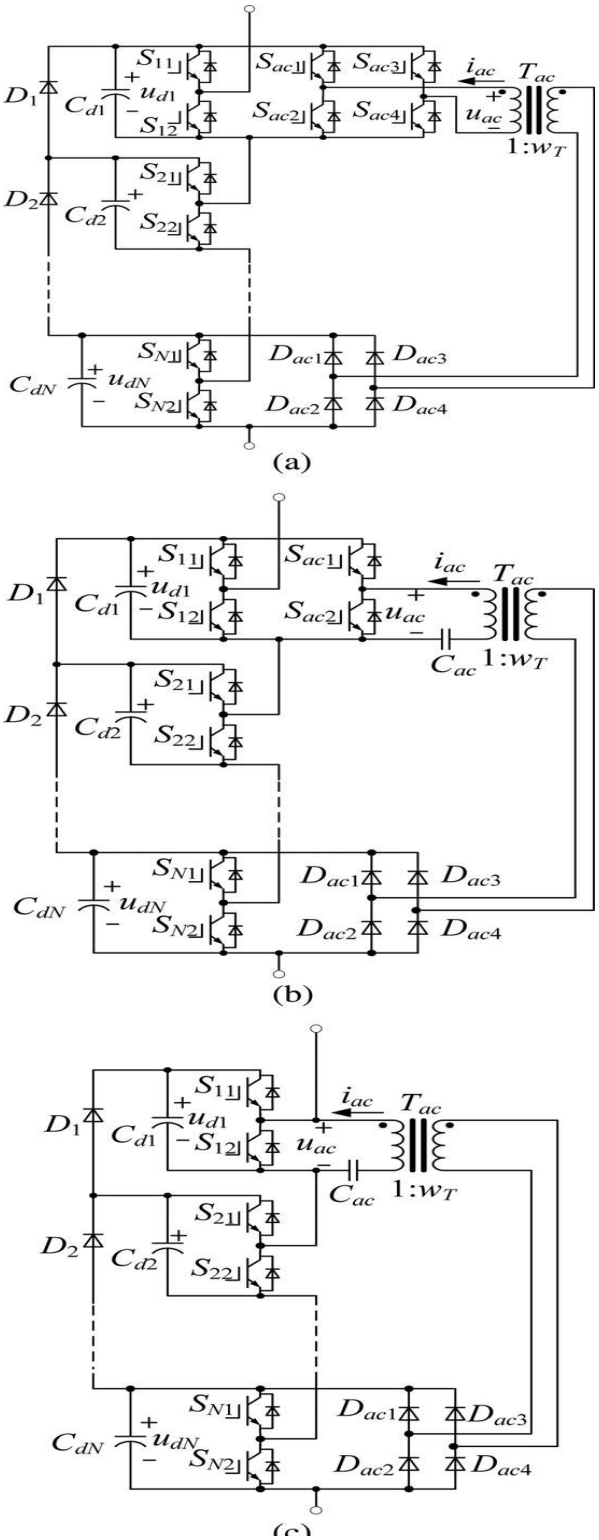

Fig. 4.Three kinds of feedback topologies. (a) Circuit based on AFBI (UCT).(b) Circuit based on AHBI (UCT). (c) Circuit based on SHI (UCT).

TABLE I
SUMMARY OF THREE AUXILIARY CIRCUITS

Type	Advantages	Disadvantages
AFBI	Independent of the main circuit Flexible control	Switch number is high Require additional control circuit.
AHBI	Fewer active switches than AFBI Independent of the main circuit Flexible control	Require additional control circuit.
SHI	Simple structure No extra active switches No extra control circuit Higher efficiency	Not independent of the main circuit

This topology requires no extra inverters or active switches; instead, the auxiliary circuit shares the two active switches with the top cell (bottom cell for DCT). The feedback circuit is composed of a transformer Tac and a rectifier connected with the secondary of Tac . The primary of Tac is also connected with a capacitor Cac for dc component blocking, and the rectifier shares one dc bus with the bottom cell (top cell for DCT).

The dc component and the low frequency components can be blocked by Cac. Usually, the frequency of the modulated wave of PWM for the main switches is low. If the feedback circuit works at the frequency of the modulated wave, the size of the transformer Tac and capacitor Cac would be quite large. Thus, the designed operating frequency of Tac is the same as the switching frequency (or the carrier frequency of PWM) of the main switches. So, the size of Tac and Cac can be significantly reduced. The core of Tac should be designed with anti saturation capability. The winding ratio (1:wT) of Tac is 1:2.

The advantages and disadvantages of the three auxiliary circuit topologies discussed previously are summarized in Table I. The working principles of the auxiliary circuits are similar, and the following part will focus on the SHI which is applied in the three-phase DCM^{2}C as a CS-APF in this paper.

B. Analysis of the Auxiliary Circuit (SHI)

The function of the feedback circuit is to transmit energy from cell 1 to cell N. The switching frequency component of the output voltage uac of cell 1 should be transmitted from the primary of Tac to the secondary, while the low frequency components should pass Lm easily and be blocked by the capacitor Cac . Lm is the magnetic inductance of Tac . The equivalent circuit of the auxiliary circuit (SHI) is shown in Fig. 5.**U**ac ,**U**Cac,**U**T 1 ,**U**T 2 , **I**ac1, and **I**ac2 are all phasors. Lσ1 and Lσ2 are the leakage inductance of the primary and secondary, respectively. **U**, T 2 , **I**, ac2 , and **L**, σ2 are referred to the primary. The total leakage inductance is Lσ = **L**σ1+ L' σ2. It should be designed as Lσ ≤ 0.1Lm. Then, the no-loading voltage of

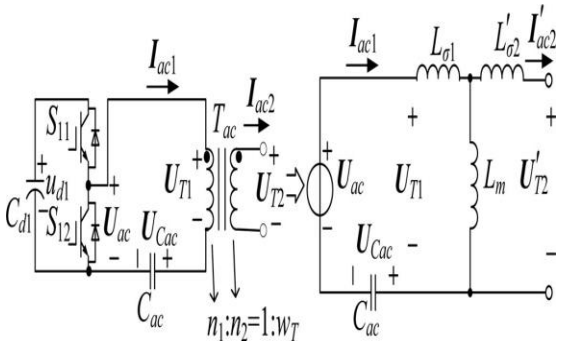

Fig.5.Equivalent circuit of the auxiliary circuit (SHI)

Tac $U_{T\ 1}$ and the capacitor voltage $\mathbf{U}_{Cac}$ may be expressed as

$$U_{T1} \approx \frac{U_{ac}\omega L_m}{\omega L_m - (1/\omega C_{ac})}, \quad U_{Cac} \approx \frac{-U_{ac}(1/\omega C_{ac})}{\omega L_m - (1/\omega C_{ac})} \tag{1}$$

Where ω is the frequency. The following expression should be Satisfied when the circuit is designed:

$$\omega_s L_m \geq \frac{10}{\omega_s C_{ac}} \tag{2}$$

Where ω_s is the switching frequency. Then, $\mathbf{U}_{T\ 1\ s} \approx$ **U**acs . **U**T 1 s and **U**ac s are the switching frequency components of **U**T 1 and **U**ac, respectively. Furthermore, it is easy to satisfy the following expression:

$$10\omega_f L_m \leq \frac{1}{\omega_f C_{ac}}. \tag{3}$$

Thus, **U**Cacf ≈**U**acf.**U**Cacf and **U**ac f are the fundamental components of **U**Cac and Uac, respectively. ωf is the fundamental frequency (frequency of the modulated wave). When Tac is loaded, there will be switching frequency ripples

ΔuCac on Cac , and the capacitor Cac should be designed to satisfy the following expression

$$\Delta u_{Cac} \le 0.1 u_{d1}. \quad (4)$$

According to (1)–(4), the relationship of uCac, uac , and uT a1 could be shown in Fig. 6. ucar is the carrier waveform with the amplitude of Umcar and um is the modulated waveform with the amplitude of Umm.

The capacitor voltage uCac approximately equals to the sum of the fundamental component and dc component, as shown in (5). Equation (6) is the control aim

$$u_{Cac} \approx D u_{d1} \quad (5)$$

$$u_{dN} \approx u_{d1}. \quad (6)$$

D is the duty cycle of the drive signal of S11 which is interlocked with S12.

Then, the expression of the current iac2 can be derived, with which the output power of the auxiliary circuit can be calculated approximately. Since the switching equency is much higher than the fundamental frequency, um and uCac can be taken as constant in a switching cycle. Thus, the expression of iac2 in a switching cycle can be derived, as shown in Fig. 7.

Ts is the switching cycle. During time 0–t1, uT 1 is

$$u_{T1} = u_{d1} - u_{Cac} \approx u_{d1} - D u_{d1}, \ (0 \le D < 0.5). \quad (7)$$

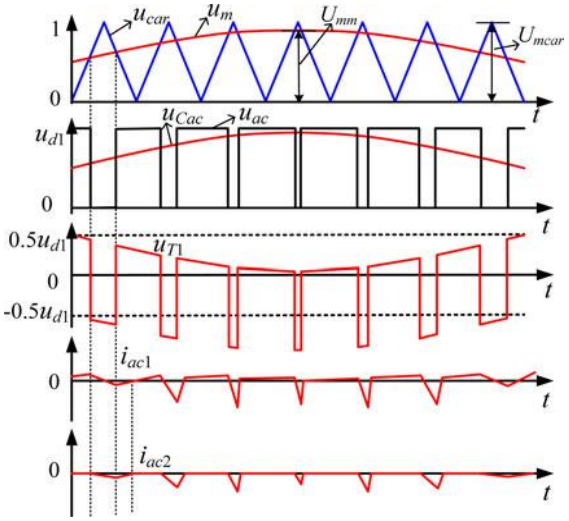

Fig.6. Relationship of the voltages uC ac , ua c, uT a1 and the currents Iac1 , Iac2 .

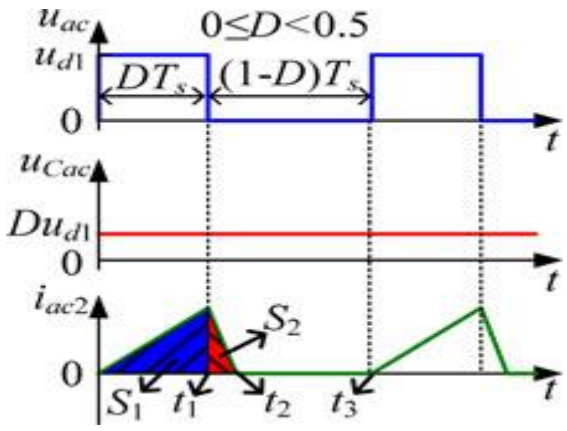

Fig. 7. Relationship of the output voltage uac and the current iac2 in the steady state of the SHI.

The secondary voltage of Tac (uT 2) can be expressed as Follows if the secondary circuit is open:

$$u_{T2} \approx w_T u_{T1} = w_T (u_{d1} - D u_{d1}) \quad (8)$$

$$\xrightarrow{0 \le D < 0.5, w_T = 2} u_{T2} > u_{d1} = u_{dN}. \quad (9)$$

Since the secondary circuit is closed, the current Iac2 will rise From time 0 to t1 according to the following expression:

$$i_{ac2}(t) \approx \frac{1}{w_T^2 L_\sigma} \int_0^t (w_T u_{T1} - u_{dN}) dt$$

$$\xrightarrow{\text{Equation(6),(7)}} = \frac{u_{d1}}{w_T^2 L_\sigma} \int_0^{DT_s} [w_T (1 - D) - 1] dt, \quad (0 \le t \le t_1). \quad (10)$$

From time t1 to t2, uac becomes zero, and u_T 1 is

$$u_{T1} = 0 - u_{Cac} \approx -D u_{d1}. \quad (11)$$

At the same time, the current iac2 will drop, and the expression is

$$i_{ac2}(t) \approx \frac{-u_{d1}}{w_T^2 L_\sigma} \int_{t_1}^t (w_T D + 1) dt, \quad (t_1 \le t \le t_2). \quad (12)$$

The rising rate δi1 of iac2 during time 0 to t1 and the falling rate δi2 during time t1 to t2 are

$$\delta_{i1} = \frac{u_{d1}[w_T (1 - D) - 1]}{w_T^2 L_\sigma}, \quad \delta_{i2} = \frac{u_{d1}(w_T D + 1)}{w_T^2 L_\sigma}. \quad (13)$$

When D <0.5, δi1 < δi2 . Thus, iac2 will fall to zero before the end of each cycle and will start from zero at the start of each cycle (iac2 = 0, t = 0) in the steady state. Then, the expression of iac2 could be obtained

$$i_{ac2}(t) \approx \frac{u_{d1}[w_T(1-D)-1]}{w_T^2 L_\sigma} t, \quad (0 \le t \le t_1). \qquad (14)$$

When D >0.5, the case is similar, but D should be replaced by 1−D in the aforementioned expressions. Besides, iac2 ≈ 0, when D = 0, D = 0.5, or D = 1 (wT = 2, ud1 = udN).

The relationship between D and iac2 is shown in Fig. 6, where uac = D·ud1 . Thus, the integration of iac2 in a duty cycle can be expressed as follows:

$$\int_0^{t_2} i_{ac2}(t)dt = S_1 + S_2 \qquad (15)$$

Where S1 and S2 are the areas of the shadows (integration of iac2) in Fig. 7. Thus, S1 :S2 = (t1−0):(t2−t1) = δi2 :δi 1 .

Then, the following expression could be obtained:

$$\int_0^{t_2} i_{ac2}(t)dt = S_1 + S_2 = \frac{\delta_{i1}+\delta_{i2}}{\delta_{i2}} \int_0^{t_1} i_{ac2}(t)dt. \qquad (16)$$

The power is the product of voltage and current as follows:

$$P(t) = u_{dN} \left| i_{ac2}(t) \right| \approx u_{d1} \left| i_{ac2}(t) \right|. \qquad (17)$$

The energy (ET s in a switching cycle Ts can be calculated, as shown in the following equations:

$$\begin{aligned} E_{Ts} &= \int_0^{T_s} P(t)dt \approx u_{d1} \int_0^{t_2} |i_{ac2}(t)|\,dt \\ &= u_{d1} \frac{\delta_{i1}+\delta_{i2}}{\delta_{i2}} \int_0^{t_1} i_{ac2}(t)dt \\ &= \frac{u_{d1}^2}{w_T^2 L_\sigma} \left[1 + \frac{w_T(1-D)-1}{1+w_T D}\right] \\ &\quad \times \int_{t=0}^{DT_s} [w_T(1-D)-1]tdt \\ &= \frac{u_{d1}^2 T_s^2 D^2 [w_T(1-D)-1]}{2w_T L_\sigma (1+w_T D)} \qquad (18) \\ &\xrightarrow{w_T=2} = \frac{u_{d1}^2 T_s^2 D^2 (1-2D)}{4L_\sigma (1+2D)}, \quad (0 \le D < 0.5). \qquad (19) \end{aligned}$$

The average power (PT s of SHI in a switching cycle is

$$P_{Ts} = \frac{E_{Ts}}{T_s} = \frac{u_{d1}^2 T_s D^2 (1-2D)}{4L_\sigma (1+2D)}. \qquad (20)$$

Then, the maximum value of PT s could be obtained with the Following expression:

$$\frac{dP_{Ts}}{dD} = \frac{d}{dD}\left[\frac{u_{d1}^2 T_s D^2 (1-2D)}{4L_\sigma (1+2D)}\right] = 0 \rightarrow D = \frac{\sqrt{5}-1}{4}. \qquad (21)$$

Similarly, D is replaced by 1−D when D ≥ 0.5. The relationship of PT s and D is given in Fig. 8, and max(PT s) can be used to design the parameters of SHI.

C. Design Rules of the Auxiliary Circuit (SHI)

Considering that the voltage unbalance between cells is mainly caused by the loss difference and the non ideal drive pulses, the required power for balance control is usually lower than 5% of the rated power cell.

Thus, the current of the clamping diode in the DCM^{2}C is lower than 5% of the rated current of the main circuit. However, 20% of the IGBT's rated current is chosen as the diode rated current for a reliable design. Of course, the diode should be fast recovery diode and have the same voltage rating as the IGBT's.

The design of SHI is focused on the auxiliary capacitor Cac and the auxiliary transformer Lm, Lσ .

According to (4), the design rules of Cac could be obtained

$$\begin{aligned} \Delta u_{Cac} &= \frac{1}{C_{ac}} \int_0^{T_s} i_{ac1}(t)dt \\ &\approx \frac{1}{C_{ac}} \int_0^{T_s} w_T i_{ac2}(t)dt = \frac{w_T}{u_{d1} C_{ac}} \int_0^{T_s} P(t)dt \qquad (22) \\ &\frac{w_T}{u_{d1} C_{ac}} \int_0^{T_s} P(t)dt \le \frac{w_T T_s \max(P_{Ts})}{u_{d1} C_{ac}} \le 0.1 u_{d1} \qquad (23) \\ C_{ac} &\ge \frac{20 T_s \max(P_{Ts})}{u_{d1}^2}, \quad (w_T = 2). \qquad (24) \end{aligned}$$

Similarly, the design of the leakage inductance Lσ can be Based on the following expression:

$$\xrightarrow{\text{Equation(20)}} L_\sigma \approx \frac{u_{d1}^2 T_s D^2 (1-2D)}{\max(P_{Ts}) 4(1+2D)}. \qquad (25)$$

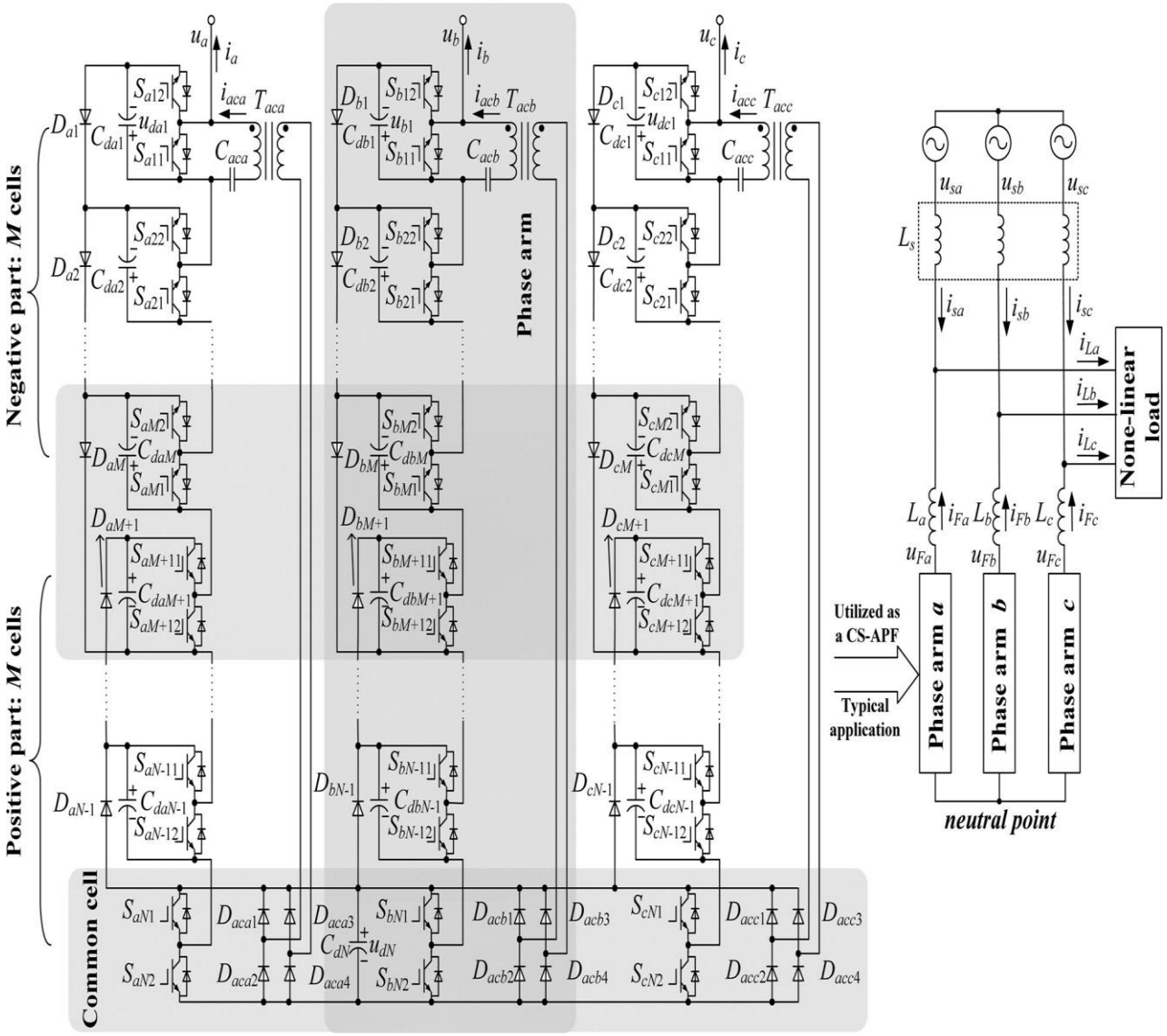

Fig.9. Topology of a three-phase converter based on DCM^{2}C (N = 2M)

$$10\omega_f \le \frac{1}{\sqrt{L_m C_{ac}}} \le 0.1\omega_s. \quad (26)$$

Similarly for Lσ

$$10\omega_f \le \frac{1}{\sqrt{L_\sigma C_{ac}}} \le 0.3\omega_s. \quad (27)$$

According the aforementioned expressions, max(PT s) should be confirmed first.

In fact, the duty cycle D changes in a sinusoidal way with t approximately, and the detailed analysis of the power is presented in Section IV. The power of SHI can be designed according to the following expression:

$$\max(P_{Ts}) \approx 1.2\max(P_{Tline}),\ \max(P_{Tline}) \approx \eta \cdot P_{cell} \quad (28)$$

Where Pcell is the rated power of a cell and PT line is defined by (39). η is approximately 3–5%.

The following section will present the topology of a three phase DCM^{2}C which can be applied in var compensation or harmonics suppression.

III. THREE-PHASE DCM^{2}CWITH STAR CONFIGURATION

A. Three-phase converter topology based on dcm^{2}c

Delta configuration and star configuration are two common choices for a cascade converter. Because the number of the cascade cells of the star configuration is smaller than that of the delta configuration for the same voltage level application, the star configuration is chosen here for discussion.

The proposed topology of a three-phase DCM^{2}C is shown in Fig. 9.It contains three phase arms for phase a, phase b, and phase c, respectively, with the same structure. The three arms are connected to a common neutral point. The converter is directly connected to a medium voltage network via three inductors without a transformer.

2M cells are connected in series in each phase arm, and divided into two parts: the positive part and the negative part, by which the positive and negative voltages are generated, respectively. Thus, the topology is a 2M+1-level converter. The UCT is arm is connected with the feedback circuit (SHI).

The three bottom cells (or the common cell of the three used for the cells in the positive part and the DCT for the negative part; thus, the common-mode voltage at the neutral point (taking the ground or the neutral point of the network as zero potential) will be reduced for easing the insulation. The top cell of each phase phases) share a common dc bus which is also shared by the three rectifiers of the feedback circuits.

The common cell provides energy exchange channels between the three phases which is beneficial to the dc-link voltage balance among three phases and also has the merits in reduction of the required number of voltage sensors. As a result, only four dc-link voltage sensors are required, and placed at the top three cells and the bottom cell for the system control.

B. Efficiency analysis of the proposed topology

There is no auxiliary circuit in the traditional cascade multilevel topologies and the capacitor voltage balance control is done by the software, while the proposed topology, DCM^{2}C, is equipped with clamping diodes and there will be current flowing through them. Thus, the efficiency of a DCM^{2}C is a little lower than that of the traditional topology.

In fact, the current flowing through the clamping diodes and the auxiliary circuit is much lower than the rated current of the main circuit. According to the analysis in Section II, the capacitor voltage unbalance is caused by the loss difference and the non ideal drive signals, and so on; thus, the power for equalizing the capacitors between two cells is usually not higher than 5% of Pcell. Then, if the total power of the clamping circuit Pe is 5% of the system's rated power Pr and the efficiency of the clamping circuit is 90%, the loss Ploss e of the clamping circuit could be calculated as follows:

$$P_{\text{loss\_}e} \approx 0.05 \times (1 - 0.9) \times P_r = 0.5\% P_r. \qquad (29)$$

In fact, the clamping circuit will not run at the maximum power point all the time. Thus, the average loss of the clamping circuit will be lower than (29). Therefore, the clamping circuit has little influence on the system efficiency in the steady state.

C. Summary of the proposed topology

Generally speaking, the proposed topology has the merits in the following aspects:

1. the capacitor voltages of the dc link are self-balanced, and the capacitor voltage balance control is completely independent from the voltage and current of the main circuit;
2. only four dc-link voltage sensors are required in the topology. The measurement and control circuit is simple;
3. the auxiliary circuit control algorithm is simple and takes up little time for calculation and the complex control algorithm can be implemented with this topology for high performance;
4 the power rating of the clamping diodes and the feedback circuit is very low. Thus, it is of low cost;
5 since the power rating of the auxiliary circuit is low, it has little influence on the system efficiency.

IV. CONTROL OF A DCM^{2}C AS A CS-APF

Applied as a CS-APF, the proposed topology based on DCM^{2}C (see Fig. 9) is discussed in the following aspects in this section:

1) Harmonic detection and compensation control;
2) Current loop control;
3) DC-link voltage control: phase arm dc-link voltage control and auxiliary clamping circuit control;
4) Modulation method.

A. Harmonic Detection and Suppression Control

Since the capacitor voltage balance is done by an auxiliary circuit, the digital controller has more time to realize a complex control algorithm, as Fig. 10 shows. The harmonics suppression control includes a load current feed-forward control and a source current feedback control [32].

In the feedback control loop, a selective harmonic detection method based on bandpass filters is used to improve the control precision with little influence on the stability.

The source currents (isa, isb, isc) are transformed into αβ coordinates. i∗ shα and i∗ shβ are the harmonic components of the source current. The controllers for the feedback control are two P regulators. C32 and C23 are the Clarke transformation and the inverse Clarke transformation

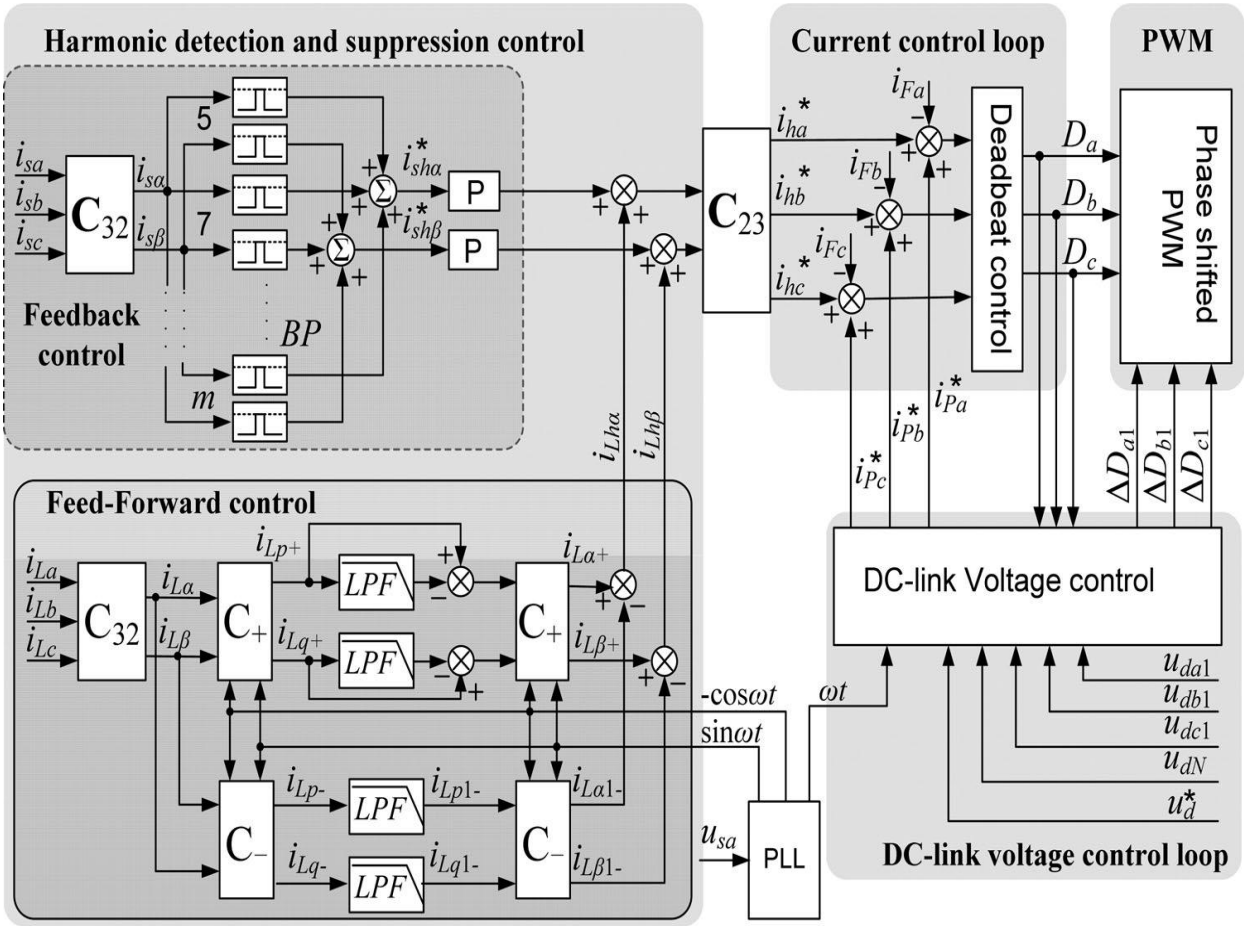

Fig.10. Control scheme of a CS-APF based on DCM^{2}C

$$\mathbf{C}_{32} = \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \quad (30)$$

$$\mathbf{C}_{23} = \begin{bmatrix} 1 & 0 \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix}. \quad (31)$$

The harmonic detection method for feed-forward control is based on the famous instantaneous reactive power theory for an improved dynamic response. The load currents (isa, isb, isc) are transformed into αβ coordinates (iL α, iLβ). iLα and iLβ are then transformed into the positive-sequence pq coordinates (iLp+, iLq+) where the positive-sequence fundamental components become dc components. The positive-sequence fundamental components are filtered out by low-pass filters and subtracted from iLp+ and iLq+. iLα and iLβ are also transformed into the negative-sequence pq coordinates (iLp−, iLq−) where the negative-sequence fundamental components become dc components and are filtered out by filters. The harmonic current, iLhα (or iLhβ), is obtained when iLα1− (or iLβ1−), the output of the inverse pq− transformation, is subtracted from iLα+ (or iLβ+), the output of the inverse pq+ transformation. Thus, the harmonic detection of the load currents is realized.

The outputs of the harmonic detection and control loop are the reference currents i∗ ha, i∗ hb, and i∗ hc **C**+ and C− in Fig. 10 are a The harmonic detection method for feed-forward control is based on the famous instantaneous reactive power theory for an improved dynamic response.

The load currents (isa, isb, isc) are transformed into αβ coordinates (iL α, iLβ). iLα and iLβ are then transformed into the positive-sequence pq coordinates (iLp+, iLq+) where the positive-sequence fundamental components become dc components. The positive-sequence fundamental components are filtered out by low-pass filters and subtracted from iLp+ and iLq+. iLα and iLβ are also transformed into the negative-sequence pq coordinates (iLp−, iLq−) where the negative-sequence fundamental components become dc components and are filtered out by filters. The harmonic current, iLhα (or iLhβ), is obtained when iLα1− (or iLβ1−), the output of the inverse pq− transformation, is subtracted from iLα+ (or iLβ+), the output of the inverse pq+ transformation.

Thus, the harmonic detection of the load currents is realized. The outputs of the harmonic detection and control loop are the reference currents i∗ ha, i∗ hb, and i∗ hc . **C**+ and C− in Fig. 10 are as follows:

$$\mathbf{C}_{+} = \begin{bmatrix} \sin\omega t & -\cos\omega t \\ -\cos\omega t & -\sin\omega t \end{bmatrix}, \quad \mathbf{C}_{-} = \begin{bmatrix} \cos\omega t & -\sin\omega t \\ \sin\omega t & \cos\omega t \end{bmatrix} \quad (32)$$

B. Current Loop Control Method

Deadbeat control which is easy to be realized by the digital controller is used as the current controller. i F (i∗ F a, iF b, iF c) is the reference current for CS-APF; ih (iha, ihb, ihc) is the harmonic reference current; and iP (iP a, iP b, iP c) is the active power reference current generated by the dc-link voltage control loop

$$i_F^* = i_h^* + i_P^*. \quad (33)$$

The phase voltage output of the converter is uF (uF a, uF b, uF c), and the source voltage is us (usa, usb, usc). udj is the dc-link capacitor voltage. Then, the expressions of deadbeat control are

$$u_F(k) = \frac{L_F}{T_s}[i_F^* - i_F(k)] + u_s(k), \quad i_F^* = i_F(k+1) \quad (34)$$

$$D = u_F \Big/ \left[\sum_{j=1}^{M} \frac{(u_{dj} + u_{dM+j})}{2}\right] \quad (35)$$

$$\times \sum_{j=1}^{M} \frac{(u_{dj} + u_{dM+j})}{2} = M \times u_{dav}$$

$$\approx \frac{M}{2}(u_{d1} + u_{dN}).$$

(36)

LF (LF a, LF b, LF c) is the inductance of CS-APF; Ts is the control cycle; D is he duty cycle; udj (j = 1, 2,. . ., M) is the cell voltages and udav is the average value of the dc-link cell voltages and udav is the average value of the dc-link voltage of a phase arm. Voltage of a phase arm.

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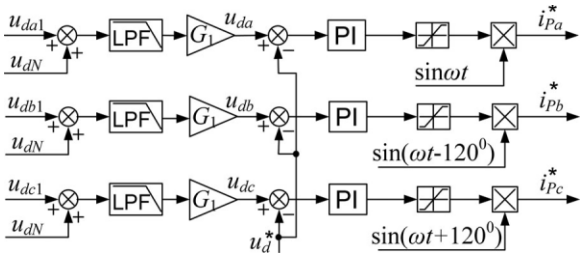

Fig. 11. DC-link voltage control scheme.

C. DC-Link Voltage Control

The dc-link voltage control includes the universal dc-link voltage control (or phase arm dc-link voltage control) and the auxiliary circuit control. Fig. 11 shows the universal dc-link voltage control scheme where u∗ d is the reference voltage, and uda, udb , and udc are, respectively, the sum of the dc-link voltage in the relevant arm of phases a, b, and c. Since only the top and bottom cells' dc-link voltage is monitored by the voltage sensors, uda can be calculated by (37) approximately. G1 is the gain in (37). Similarly, udb and udc can be calculated. The errors are the inputs of the proportional-integral regulators. The outputs of the regulators are multiplied by the phase-locked loop signals. Thus, the outputs of the universal dc-link voltage control are the active power reference currents (i P a, iP b, iP c) for each phase

$$u_{da} = \sum_{j=1}^{M} u_{dj} \approx G_1(u_{da1} + u_{dN}) = \frac{M}{2}(u_{da1} + u_{dN}). \quad (37)$$

The dc bus of the common cell is shared by the three phases. Thus, certain amount of energy can be exchanged among the three phases which is beneficial for the dc-link voltage balance of the three phases

The dc-link voltages of the cells are balanced by the auxiliary clamping circuit, and the control principle is described as follows (take phase arm a for example).

According to the analysis in Section II, the equalizing of the

capacitor voltages focuses on the control of the feedback circuit (SHI).

The aim of the control is that the capacitor voltage of cell 1 is clamped near to the capacitor voltage of cell N. The output power of the feedback circuit (SHI) actually changes with the duty cycle D. Thus, the power control of the feedback circuit can be realized by adjusting the duty cycle of the top cell, and it should not affect the performance of the main circuit.

In fact, the major low-frequency component of ua1 (uac in Section II) is the line frequency component which is determined by the modulated wave (see Fig. 16). So, the energy ET line output by the feedback circuit in a line voltage cycle Tline is

$$E_{T\text{line}} = \int_0^{T_{\text{line}}} P(t)dt. \quad (38)$$

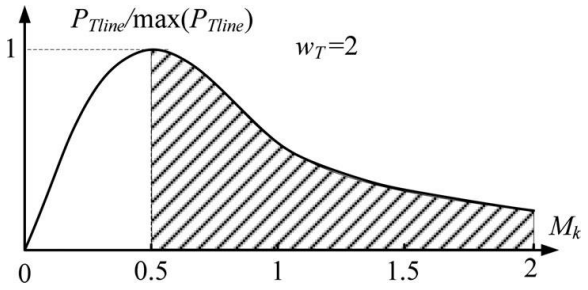

Fig.12. Relationship between the energy *ET Line* and *Mk* .

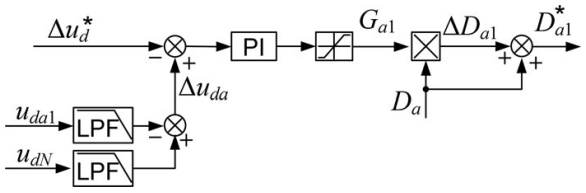

Fig13. Control scheme of the auxiliary circuit.

The average power of the auxiliary circuit PT line is

$$P_{T\text{line}} = \frac{E_{T\text{line}}}{T_{\text{line}}}. \quad (39)$$

The specific expression of PT line can be derived according to (12), (17), (38), and (39). Besides, D is expressed in (40), where ωline is the line frequency

$$D \approx 0.5[M_k \sin(\omega_{\text{line}} t) + 1] \quad (40)$$

$$M_k = U_{mm}/U_{mcar}. \quad (41)$$

The expression of PT line is very complex. The relationship between PT line and the modulation index Mk can be obtained

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by simulation and a simulation result is shown in Fig. 12 (Wt = 2). Mk ≤ 1 means the modulation is normal, and Mk ≥1 means the switch holds (without switching) for a while during half a line voltage cycle (over modulated).

The curve of Fig. 12 shows that when Mk ≥ 0.5, the trend of PT line is monotonic decreasing. Then, the feedback circuit can be controlled in this region (within the shadows). Thus, the control for power transmission from cell 1 to cell N can be realized by adjusting the modulation index of cell 1, and the control scheme of the clamping circuit is shown in Fig. 13. Δuda is the difference between uda1 and U_{DN}. When Δuda exceeds the reference value Δu∗ d,Ga1 will increase, while the transmitted power will decrease.

Similarly, the transmitted power will increase as Δuda decreases. Taking the voltage drop of the clamping diode and the saturation voltage of the IGBT into consideration, Δu∗ d may be assigned with a value slightly greater than 0.

The output voltage of the cell 1 will change ifDa1 is adjusted by ΔDa1 . Thus ,the voltage should be compensated by the other cells of phase a (see Fig. 17).

D. Modulation Method

The number of the cells of the positive part equals to that of the negative part. Although the proposed topology is based on the half-bridge inverter, a pair of half-bridges (one positive cell and one negative cell) can be controlled together. Thus, cell j (1 ≤ j ≤ M) and cell M+j can be taken as an equivalent unit or an imaginary unit from the viewpoint of modulation, as Fig. 14 shows (i.e., phase a).

Vd is the capacitor voltage. The output voltage of the equivalent unit is uo1 . The relationship of uo1 and the switch state is presented in Table III and Fig. 15.

According to Table II, Sa11 and SaM +11 could share the same modulated wave if SPWM method is applied. Among the modulation methods of the cascade multilevel converter [33]–[39], phase-shifted PWM method is easy to be realized without

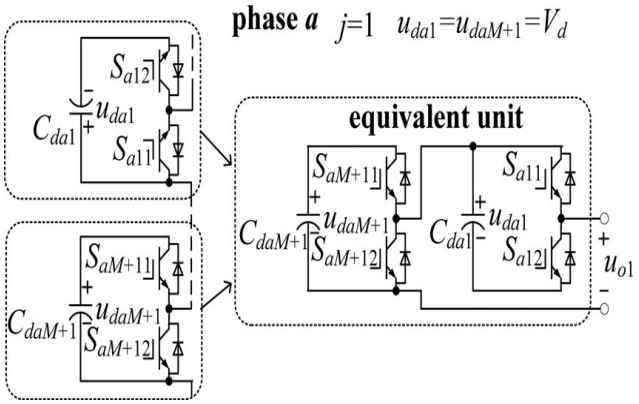

Fig.14. Equivalent unit of the two cells.

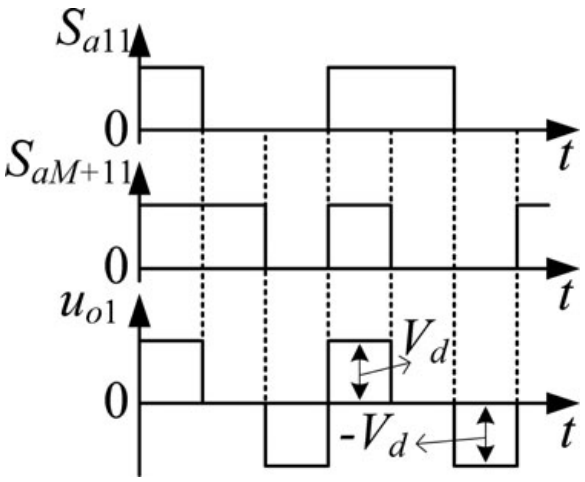

Fig.15. Relationship between the output voltage and the drive signals of the equivalent unit.

TABLE II

OUTPUT VOLTAGE OF THE EQUIVALENT UNIT AND SWITCH STATE

u_{o1}	S_{a11}	S_{a12}	S_{aM+11}	S_{aM+12}
V_d	1	0	1	0
0	0	1	1	0
0	1	0	0	1
$-V_d$	0	1	0	1

complex algorithm. Moreover, the equivalent switching frequency is very high. So, it is a good choice for DCM^2C.

Fig. 16 shows the modulation principle for a DCM^2C based on phase-shifted PWM method. M is the number of the cells in the positive part or the negative part (M is 3 in Fig. 16). Sj1 is the drive

signal for the upper switch of cell j, which is interlocked with the drive signal Sj2. The phase of the carrier of cell j leads that of cell j+M by π. The carrier phase shift between cell j and cell j+1 is

$$\Delta\theta = \frac{\pi}{M}. \qquad (42)$$

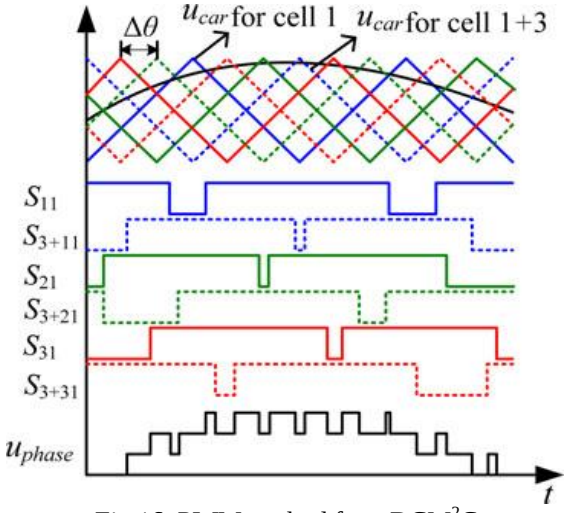

Fig.16. PWM method for a DCM^{2}C.

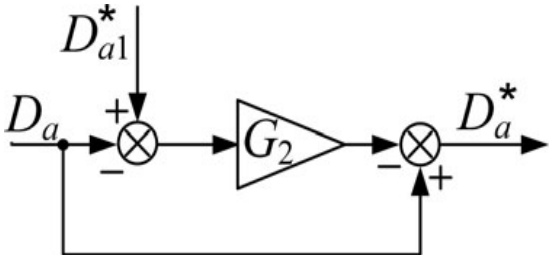

Fig.17. PWM duty adjustment.

The drive signals for the six upper switches are shown in Fig. 16. U Phase is the output voltage of a phase arm. Since the auxiliary circuit control of cell 1 will change the duty cycle, it will be better if the duty cycle control for cell 1 is independent from that of other cells in the phase arm. The PWM duty control scheme is shown in Fig. 17. D∗ a1 is the new PWM duty cycle for cell 1(see Fig. 13), and D∗ a is for the other cells of phase a.

The gain G2 is determined by the following expression:

$$G_2 = \frac{1}{2M-1}. \qquad (43)$$

V. IMPLEMENTATION OF FUZZY LOGIC CONTROLLER

In FLC, basic control action is determined by a set of linguistic rules. These rules are determined by the system. Since the numerical variables are converted into linguistic variables, mathematical modeling of the system is not required in FC. The FLC comprises of three parts: fuzzification, interference engine and defuzzification. The FC is characterized as; i. seven fuzzy sets for each input and output. ii. Triangular membership functions for simplicity. iii. Fuzzification using continuous universe of discourse. iv. Implication using Mamdani"s,, min" operator. v. Defuzzification using the „height" method.

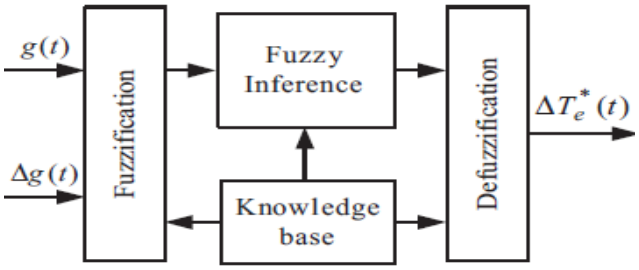

Fig.18.fuzzy Logic Controller

Fuzzification

Membership function values are assigned to the linguistic variables, using seven fuzzy subsets: NB (Negative Big), NM (Negative Medium), NS (Negative Small), ZE (Zero), PS (Positive Small), PM (Positive Medium) and PB (Positive Big). The partition of fuzzy subsets and the shape of membership function adapt the shape up to appropriate system. The value of input error *E(k)* and change in error *CE(k)* are normalized by an input scaling factor.

In this system the input scaling factor has been designed such that input values are between -1 and +1. The triangular shape of the membership function of this arrangement presumes that for any Particular input there is only one dominant fuzzy subset. The input error *E(k)* for the FLC is given as

$$E(K) = \frac{P_{pk(k)} - P_{pk(K-1)}}{V_{pk(K)} - V_{pk(K-1)}}$$

$$CE(K) = E(K) - E(K-1) \qquad (44)$$

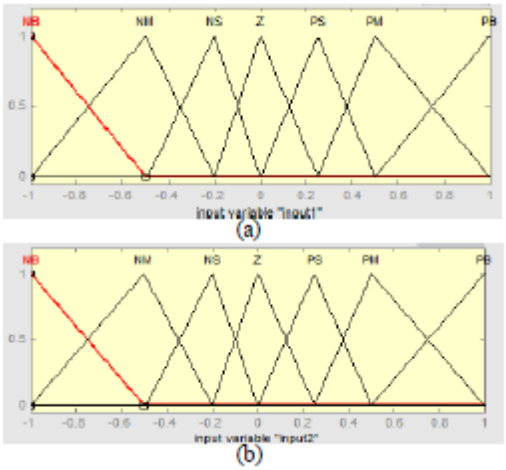

Fig.19. (a) & (b) Membership functions

Inference Method

Several composition methods such as Max–Min and Max-Dot have been proposed in the literature. In this paper Min method is used. The output membership function of each rule is given by the minimum operator and maximum operator.

Table III shows rule base of the FLC. ***Defuzzification*** As a plant usually requires a non-fuzzy value of control, a defuzzification stage is needed. To compute the output of the FLC, „height" method is used and the FLC output modifies the control output. Further, the output of FLC controls the switch in the inverter..

In order to control these parameters, they are sensed and compared with the reference values. To achieve this, the membership functions of FC are: error, change in error as shown in Figs. 19 (a), (b). In the present work, for fuzzification, non-uniform fuzzifier has been used. If the exact values of error and change in error are small, they are divided conversely and if the values are large, they are divided coarsely.

$$u = -[\propto E + (1-\propto) * c] \qquad (45)$$

Where α is self-adjustable factor which can regulate the whole operation. E is the error of the system, C is the change in error and u is the control variable.

A large value of error E indicates that given system is not in the balanced state. If the system is unbalanced, the controller should enlarge its control variables to balance the system as early as possible. One the other hand, small value of the error E indicates that the system is near to balanced state. Overshoot plays an important role in the system stability. Less over shoot is required for system stability and in restraining oscillations. C in (12) plays an important role, while the role of E is diminished. The optimization is done by α. The set of FC rules is given in Table III.

TABLE IV
FUZZY RULES

e / Δe	NB	NM	NS	ZE	PS	PM	PB
NB	NB	NB	NB	NB	NM	NS	ZE
NM	NB	NB	NB	NM	NS	ZE	PS
NS	NB	NB	NM	NS	ZE	PS	PM
ZE	NB	NM	NS	ZE	PS	PM	PB
PS	NM	NS	ZE	PS	PM	PB	PB
PM	NS	ZE	PS	PM	PB	PB	PB
PB	ZE	PS	PM	PB	PB	PB	PB

VI. SIMULATION RESULTS

A. Simulation Study with PI Controller

A simulation model of a seven-level CS-APF based on DCM^{2}C has been designed. The topology is the same as the one shown in Fig. 9, and the system control is presented in Fig. 10.

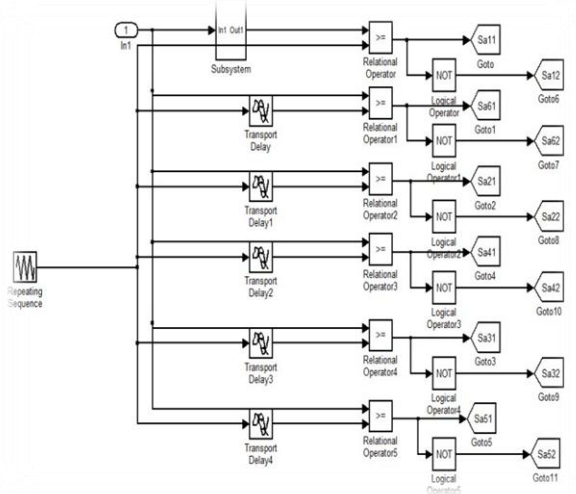

Fig.20.pulse generation for inverter switches

A resistor is connected to each cell's capacitor in parallel, and the differences of power loss between cells are simulated with different values of the resistors. Fig. 18 shows the simulation results of the proposed seven level CS-APF. The sequence of the waveforms is (from top to bottom) isa, iLa, and iF a. The distorted source current is well corrected by the CS-APF.

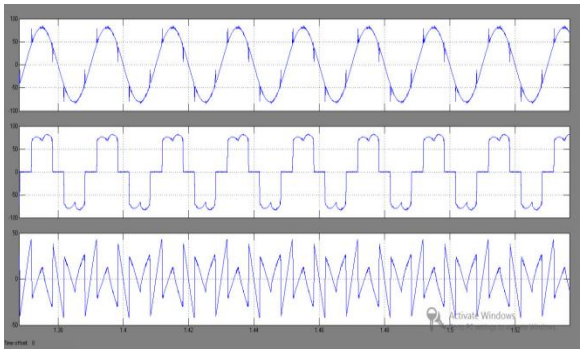

Fig.21. Simulation waveforms of isa , iLa , and iF a.

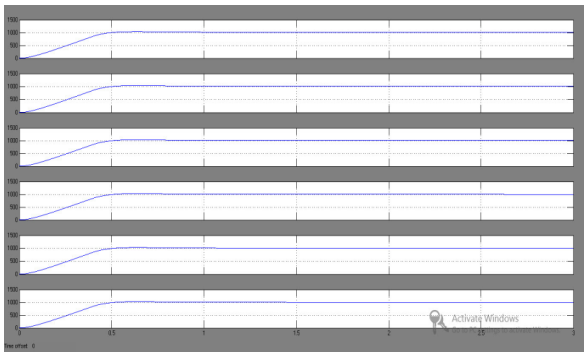

Fig.22. DC-link voltages of CS-APF (phase a) with the clamping circuit in operation.

The dc-link voltages of a seven-level CS-APF based on DCM^{2}C are presented in Fig. 22(phase a). The capacitor voltages are well balanced by the clamping circuit, and the voltage differences are not higher than 10 V. Besides, the voltage ripples of CdN are very low for the common cell shared by the three phases.

Fig. 23 shows the simulation results of the dc-link capacitor voltages of the proposed seven-level CS-APF with the energy feedback circuit turned OFF. The capacitor voltages become unbalanced. However, with the clamping diodes working, the relationship of the capacitor voltages is uda1 > uda2 > uda3 > uda4 = uda5 > udN .

Fig. 24 shows the simulation results of a seven-level CSAPF based on the basic half-bridge inverter. With no voltage balance control, the dc-link capacitor voltages gradually become unbalanced. Unlike that in the system based on DCM^{2}C, the relationship of the voltages is uda3 > uda5≈uda1 > uda2 > uda4 > udN . It is similar to the relationship of the resistance in Table IV: Ra3 > Ra1 > Ra5 > Ra2 > Ra4 > RaN

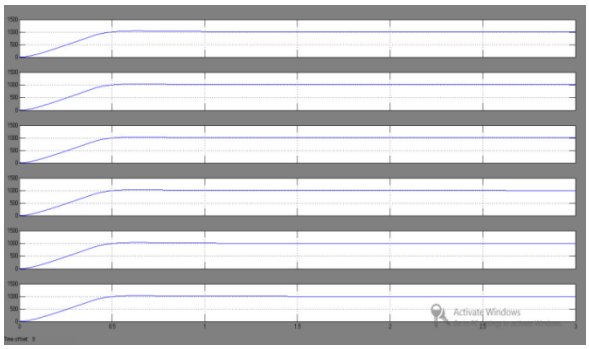

Fig.23. DC-link voltages of CS-APF based on DCM^{2}C with the energy feedback circuit turned OFF.

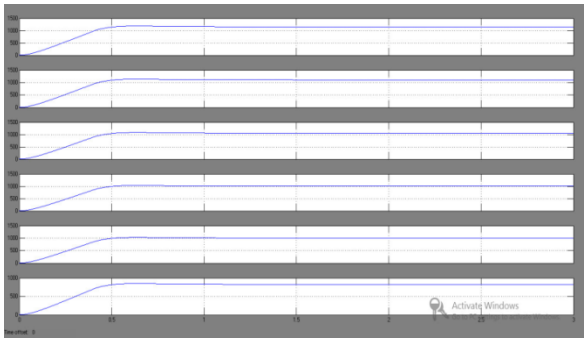

Fig.24. DC-link voltage of a CS-APF based on basic half-bridge inverter.

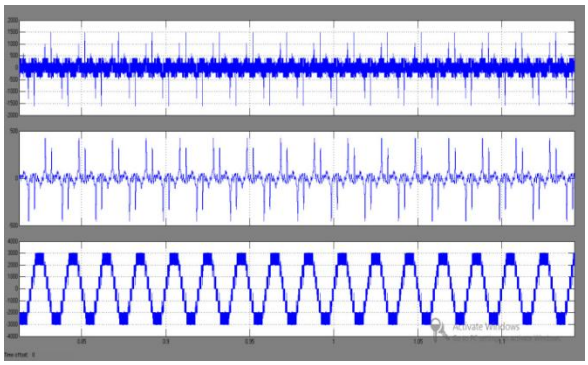

Fig.25. Common-mode voltage of the neutral point of the proposed CS-APF.

The common-mode voltage of the neutral point of a seven level CS-APF based on DCM^{2}C is shown in Fig. 27. The sequence of the waveforms is (from top to bottom) un, u_ n , and uF a. un is the voltage between the negative pole of CdN and the neutral point of the power source. It is much lower than the source voltage. u_ n is the voltage filtered from un by a low-pass filter with the cutoff frequency of 1 kHz. u_n is lower than 200 V. uF a is the voltage of phase arm a of the CS-APF, and is seven-level voltage.

B. Simulation network with fuzzy logic controller

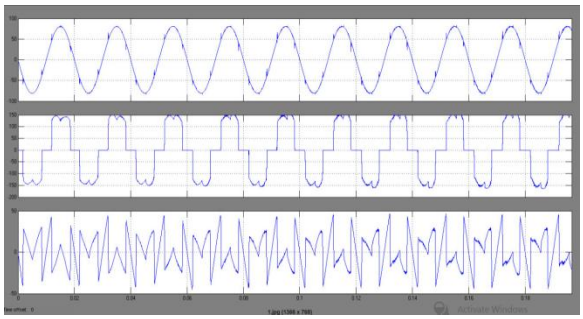

Fig.26. Simulation waveforms of isa , iLa , and iF a .

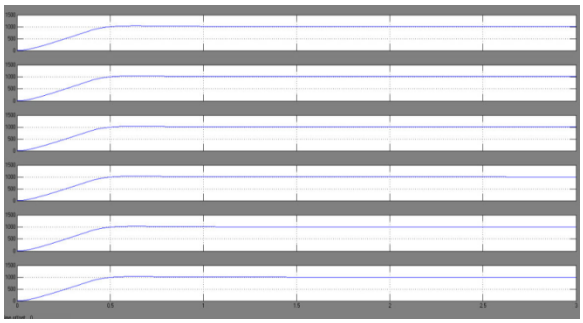

Fig. 27. DC-link voltages of CS-APF (phase a) with the clamping circuit in operation.

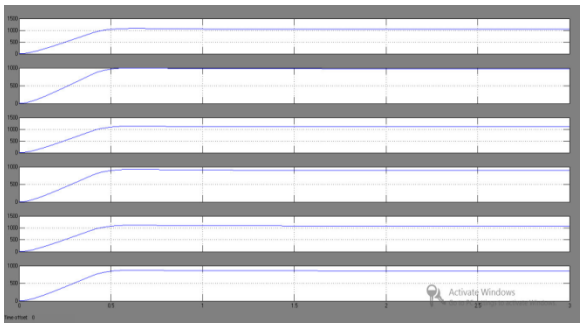

Fig.28. DC-link voltages of CS-APF based on DCM^{2}C with the energy feedback circuit turned OFF.

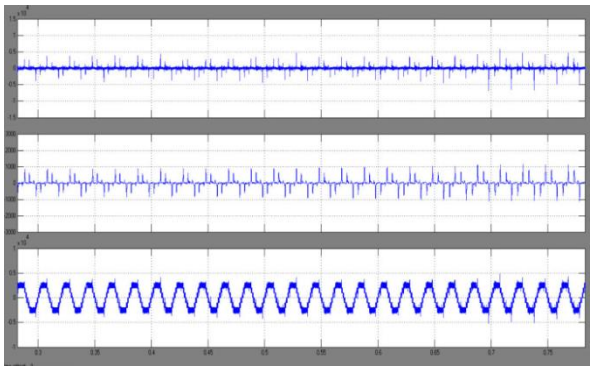

Fig.29.Common-mode voltage of the neutral point of the proposed CS-APF.

VII. CONCLUSION

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A novel topology of a DCM^{2}C is proposed in this paper using fuzzy logic controller. The topology is proved to be a suitable solution for high-voltage and high-power application instead of using pi controller. Voltage balance for all dc-link capacitors is realized with a proposed simple feedback auxiliary circuit. The number of dc-link voltage sensors could be decreased significantly, and also the transient time interval and study state time interval gets reduced which reduces control complexity and system cost. Three kinds of auxiliary circuits are resented and analyzed in this paper.

The novel topology of a three-phase DCM^{2}C with the auxiliary circuits (SHI) is applied as a CS-APF, and the system control algorithm and specific mathematical model are presented. With only four voltage sensors at the dc-link side, the dc-link voltages are well balanced. Furthermore, the complexity of the system control algorithm does not increase with the number of cells increasing. The system can operate under normal condition even only one phase auxiliary circuit is in operation. So, the reliability of dc-link voltage balance is significantly enhanced. With simple topology, perfect clamping performance, and very small number of voltage sensors, a DCM^{2}C is a perfect solution for medium-/high-voltage applications. It can be useful in many applications, such as HVDC, STATCOM, etc.

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