



Comparison of Several MLI Topologies Fed Brushless DC Machine Drive System

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Abstract:

In this a novel seven inverter with lesser number of switches encouraged to BLDC engine drive is proposed. In a normal Brush Less DC engine (BLDC) drive, the engine when all is said in done bolstered with Pulse width tweaked (PWM) voltages which cause sudden voltage wave fronts (dv/dt) to happen over the engine terminals. This may potentially go with the engine protection stoppage. Also, engine harms are accounted for because of the high-voltage change rates (dv/dt) which delivers basic mode voltages at the engine windings. For variable-speed medium-voltage drives this is a bit of huge concern where the voltage levels are exceedingly far over the ground. The normal issue can be determined by applying variable voltage with low dv/dt i.e., making the utilization of multilevel inverter. In this proposed topology, power cells connected in course utilizing two inverter legs as a part of arrangement, as an option of two parallel inverter legs, set up in CHB power cells, routinely. In this proposed topology info voltage is $V_{dc}/2$ just. So that seriousness of blast is decreased to half and results in expansion of the framework's dependability and savvy. Nitty gritty examinations of the proposed structure with five levels are done utilizing heartbeat width regulation stage moved multicarrier balance. At last seven level Cascaded multilevel inverter bolstered Brushless dc engine drive is actualized in Matlab/Simulink and reproduction results are introduced for confirmation and approval of the proposed work. Considering the drive favorable circumstances of BLDC drive contrasted with other commute applications BLDC with stage exchanging inverter execution is enhanced with multilevel inverter(MLI)topologies utilizing present and velocity control strategies which diminish the torque swells and symphonious mutilation when all is said in done three stage three level inverter which commutates the BLDCM and location the issues of sounds and torque swells for that by utilizing a multilevel inverter topology of five level inverter with present and rate Controller at lower exchanging levels which can enhances the BLDC drive execution. This paper proposes an arrangement associated five level inverter with stage shift tweak with present and rate control methods to diminish the consonant bending

and torque swells. The recreation results are talked about with a relative study in diverse working procedures of BLDC drive. The reproduction results in view of Matlab/Simulink are talked about in point of interest in this paper. To accomplish favored level of execution the engine requires suitable controller. Perpetual magnet engines are normally using so as to accomplish the velocity control corresponding basic controller. BLDC engine drive utilizes one or more sensors giving positional data to keep synchronization. It results in a higher commute cost because of sensor wiring and execution in the engine. Likewise, sensors can't be utilized as a part of uses like the rotor is in shut lodging and the engine is submerged in a fluid. Subsequently, for expense and specialized reasons, the BLDC sensor less commute is a key ability of a brushless engine controller. Executions of sensor less BLDC control with the most reduced conceivable framework expense is fundamental for keeping up the most elevated execution. This paper demonstrates that the torque delivered by the BLDC engines with trapezoidal Back EMF is consistent under perfect condition. Because of freewheeling torque swells are delivered which are to be either wiped out or lessened. This paper proposes, a five level diode braced multilevel inverter to lessen the torque swell and the same was reproduced utilizing MATLAB programming.

Keywords: Brushless DC Motor (BLDC), Diode Clamped Multilevel Inverter, Torque Ripple, PI Controller, Sinusoidal Pulse Width Modulation (SPWM).

I. Introduction

Brushless DC Motor with trapezoidal BEMF has numerous favorable circumstances. It has high proficiency and high power thickness, unwavering quality in light of the fact that the nonappearance of field winding and brushes. So it has low support, Simple casing and grinding, high ability. Despite the fact that in a reasonable case BLDC drive have torque throbs because of Back EMF abandonment from the perfect. Torque swell produces clamor and issue of pace control. Due to Power electronic compensation, diode freewheeling of latent stages and High recurrence exchanging of force electronic gadgets, another issue is inverter yield or info of the

BLDC Motor have numerous music that will create Electromagnetic Interference. Brushless direct current (BLDC) engines have qualities of high dependability, basic casing, and little grinding. By contrasting and PMSM, BLDC engine has the benefits of rapid conforming execution and force thickness. The torque swell decrease and the control execution change of BLDC primarily centered around compensation torque swell, the torque swell created by diode freewheeling of idle stage, and the torque swell brought on by the non-perfect back electromotive power (EMF). For the recompense torque swell, Calson et al. suggested that relative torque is identified with current and differs with rate. In, a solitary dc current sensor and a versatile stage change point regulation plan ought to be utilized to smother the replacement torque swell, however the diode freewheeling of dormant stage was not considered. Chuang et al. have dissected the mastery of distinctive heartbeat width regulation (PWM) designs on the recompense torque swells as per the BLDC engines with perfect trapezoidal back EMF [6], the corresponding vital (PI) controller is a surely understood framework in control building. It is fundamentally a slack compensator portrayed by the exchange capacity. BLDC engine position can be detected from Back EMF (BEMF). It has been worked fitting exchanging of inverters. Yield rate of BLDC engine can be detected and contrasted with the reference velocity utilizing comparator. So mistake created sign is sent as information for PI controller. PI controller endeavors to right that slip between a deliberate procedure variable and wanted set point by computing and after that yielding restorative activity that can modify the procedure appropriately. The PI controller figuring includes two separate modes, the corresponding mode, and indispensable mode. The relative (KP) mode focus the response to the present mistake, essential (Ki) mode decides the response based late blunder. The weighted total of the two modes (KP and Ki) yield as restorative activity to the control component. PI (Proportional fundamental) controller is broadly utilized as a part of industry because of its straightforwardness in outline and basic structure.

Brushless DC engines, rather shockingly, is a sort of perpetual financier synchronous engine. Perpetual magnet synchronous engines are characterized on the wave's premise state of their impel emf, i.e, sinusoidal and trapezoidal. The sinusoidal sort is known as perpetual magnet synchronous engine; the trapezoidal sort goes under the name of PM Brushless dc (BLDC) machine. Lasting magnet (PM) DC brushed and brushless engines join a mix of PM and electromagnetic fields to create torque (or power) bringing about movement. In a brushless engine, the rotor consolidates the magnets, and the stator contains the windings. As the name proposes brushes are truant and consequently for this situation, replacement is actualized electronically with a drive

intensifier that uses semiconductor changes to change current in the windings taking into account rotor position input. In this regard, the BLDC engine is comparable to a switched DC commutator engine, in which the magnet pivots while the conductors stay stationary. Hence, BLDC engines regularly fuse either inner or outside position sensors to sense the genuine rotor. The BLDC engine is an AC synchronous engine with lasting magnets on the rotor (moving part) and windings on the stator (settled part). Changeless magnets make the rotor flux and the stimulated stator windings make electromagnet posts.

The rotor (proportionate to a bar magnet) is pulled in by the empowered Stator stage. By utilizing the proper arrangement to supply the stator stages, a turning field on the stator is made and kept up. This activity of the rotor, pursuing the electromagnet posts on the stator, is the crucial activity utilized as a part of synchronous perpetual magnet engines. The lead between the rotor and the turning field must be controlled to deliver torque and this synchronization suggests learning of the rotor position.

II. Diode Clamped Multilevel Inverter

A three-phase five level DC- MLI topology is shown in Fig. Each of the three-phase outputs of inverter shares a common DC bus voltage that has been divided into five levels over four DC bus capacitors. The capacitors have been subscripted from C_1 to C_4 . The middle point of C_2 and C_3 capacitors constitute the neutral point of inverter and output voltages have five voltage states referring to neutral point. The voltage across each capacitor is $V_{dc}/4$ and the voltage stress on each switching device is limited to V_{dc} through the clamping diodes that have been named as $D_{1,3}$ and D_{dc31} ¹¹. The key components that differ with this topology from a conventional two-level inverter are clamping diodes. The neutral point n has been assumed as the output phase Voltage reference and the switching combinations have been analysed for phase an output voltage V_{an} as seen in Table 1.

For the five level DC-MLI in Fig., a set of four switches is ON at any given period of time and they are S_{a1} to S_{a4} for voltage level of $V_{an}=V_{dc}/2$. The second switching state shows the voltage level of $V_{an}=V_{dc}/4$ and S_{a2} to S_{a1} switches should be triggered. The remaining switching state that constitutes zero and negative outputs can be seen in Table 1. The clamping diodes require different voltage ratings for reverse voltage blocking due to each triggered switch is only required to block a voltage level of $V_{dc}/(m-1)$. By assuming the switches from S_{a1} to S_{a4} are triggered as seen in first line of Table 1, D_1 blocking diode needs to block a voltage at the rate of $3V_{dc}/4$ that is generated by three DC bus capacitors.

Since each blocking diode voltage rating is the same as the active device voltage rating. The required number of diodes for each phase will be calculated as $(m-1)$. $(m-2)$, where m represents number of inverter levels. The following equations are used to determine the required device numbers to form a given level of a diode

clamped MLI. If m is assumed as the number of levels, the number of capacitors at the DC side (c) can be known by using Equation (1).

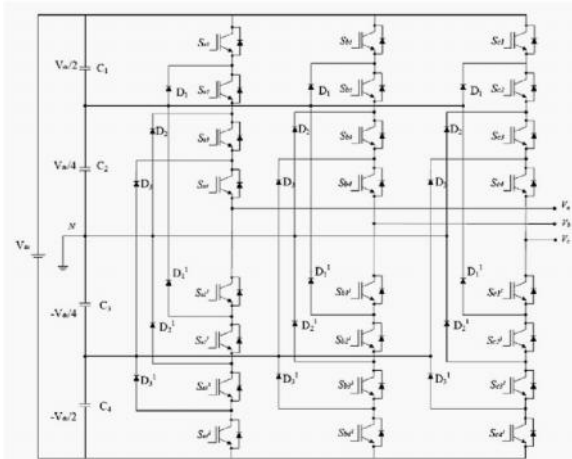


Fig.1 Three phase five level topology of diode clamped multilevel inverter

The number of freewheeling diodes (d) per phase, and the number of clamping diodes (j) can be calculated by using Equations (2) and (3) respectively.

$$c = m - 1 \quad (2)$$

$$d = 2(m - 1) \quad (3)$$

$$j = (m - 1) \cdot (m - 2)$$

Table 1 Voltage levels of five level diode clamped multilevel inverter and switching states.

Voltage V_{an}	Switching state							
	S_{a1}	S_{a2}	S_{a3}	S_{a4}	S_{c1}^1	S_{c2}^1	S_{c3}^1	S_{c4}^1
$V_4 = V_{dc}/2$	1	1	1	1	0	0	0	0
$V_3 = V_{dc}/4$	0	1	1	1	1	0	0	0
$V_2 = 0$	0	0	1	1	1	1	0	0
$V_1 = -V_{dc}/4$	0	0	0	1	1	1	1	0
$V_0 = -V_{dc}/2$	0	0	0	0	1	1	1	1

The DC-MLI are efficient in fundamental frequency switching applications but the number of clamping diodes required is quadratic ally related to the number of levels. Fundamental frequency switching will cause an increment on voltage and current THD, while increased number of clamping diode makes the topology large.

Cascaded H-Bridge MLC

A multilevel converter drive for Brushless DC motors is proposed using the cascaded H-bridge topology shown in Figure 3. The cascaded H-bridge multilevel topology isolates individual battery cells, thereby facilitating individual cell monitoring. The vehicle management system can then take SoC into account during operation, to perform charge balancing, to optimize cell performance and to initiate remedial action should a cell catastrophically fail.

The multilevel converter produces PWM output from a single cell at a time, so dv/dt is reduced, decreasing the filtering requirements and common mode and bearing currents that have been linked to mechanical failure [2, 3].

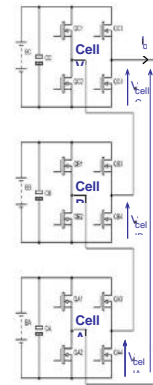


Figure.2: 7-level Cascaded H-bridge

The current ripple in the machine is also reduced, by switching a greater number of lower voltage levels, either improving the torque characteristic of the drive or allowing for the use of higher power density, lower inductance machines. When used with a BLAC motor, near sinusoidal waveforms can be generated with or without high frequency PWM.

Sources [4-6] that investigate multilevel converter performance, topologies, applications and modulation strategies agree on further fundamental advantages of the multilevel converters not specifically covered here, such as the reduced voltage stress of the switching devices and harmonic distortion with more accurately synthesized output waveforms.

In a more specific paper for this application [7], the use and analysis of a multilevel DC drive for low inductance machines is presented using the multilevel converter to modulate the DC link of a six switch inverter. However, this does not consider the effect of operation on battery SoC. The work cited in [8] specifically presents methods of balancing discharge and charge equalisation but does not include the implementation of SoC estimation. This paper will expand on ideas from each, producing reduced current ripple and charge balancing with the addition of battery management as well as SoC estimation, within a motor drive. Unequal source voltages, such as those encountered with battery packs, are considered in [9] with a method presented to calculate switching angles to minimize total harmonic distortion. The proposed drive is focussing on equalising these voltages rather than minimizing the harmonic distortion caused by the unequal sources. The cascaded multilevel converter has a natural fault tolerance, where, if any cell should fail, it can be bypassed by switching on a pair of high side or low side switches depending on the fault, and the converter will continue to operate with the output voltage reduced by only a single cell voltage.

SoC estimation will be based on observer techniques to provide an accurate SoC indication without requiring

either initial calibration, or suffering from the cumulative errors caused by integration techniques.

III. Design Of Inverter Modules

Figure 3. shows the proposed five level cascade H bridge inverter fed BLDC motor drive. Figure 4 shows single phase structure of a multilevel cascade H bridge inverter. The N-level cascaded H-bridge, multilevel inverter comprises $\frac{1}{2}(N-1)$ series connected single phase H-bridges per phase, for which each H-bridge has its own isolated dc source. Three output voltages are possible, $\pm V_s$, and zero.

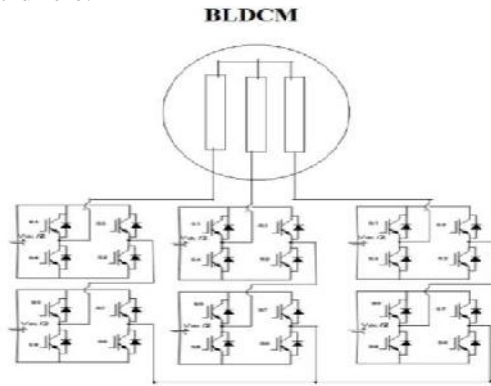


Figure 3: Proposed Five Level Cascade H Bridge Inverter Fed BLDC Motor Drive

The cascaded H-bridge multilevel inverter is based on multiple two level inverter outputs (each Hbridge), with the output of each phase shifted. Despite four diodes and switches, it achieves the greatest number of output voltage levels for the fewest switches. Its main limitation lies in its need for isolated power sources for each level and for each phase, although for VA compensation, capacitors replace the dc supplies, and the necessary capacitor energy is only to replace losses due to inverter losses. Its modular structure of identical H-bridges is a positive feature.

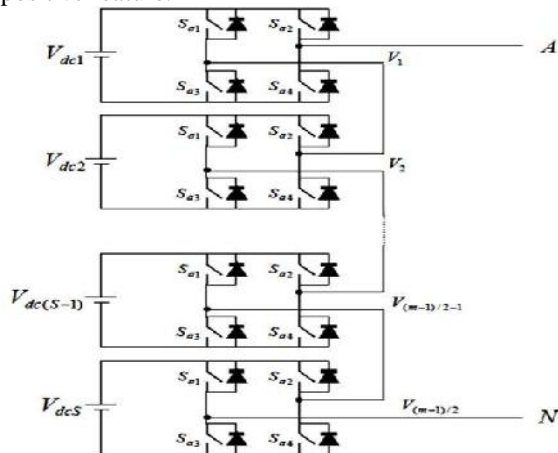


Figure 4: Single-Phase Structure of a Multilevel Cascaded H-Bridge Inverter

IV. Proposed Architecture:

The proposed BLDC drive system, shown in Figure 5, consists of three isolated H-bridge cells each with a 12V battery, phase controller, standard six-switch inverter providing commutation, and driving a BLDC 1.2 kW motor. With the six-switch inverter providing commutation, only a single phase multilevel converter is required, reducing complexity but allowing development of the battery management algorithms.

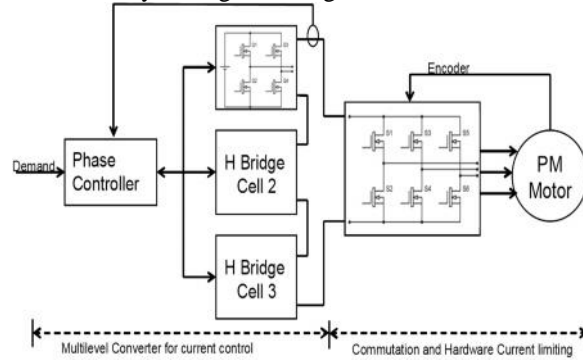


Fig 5. Proposed Multilevel BLDC line

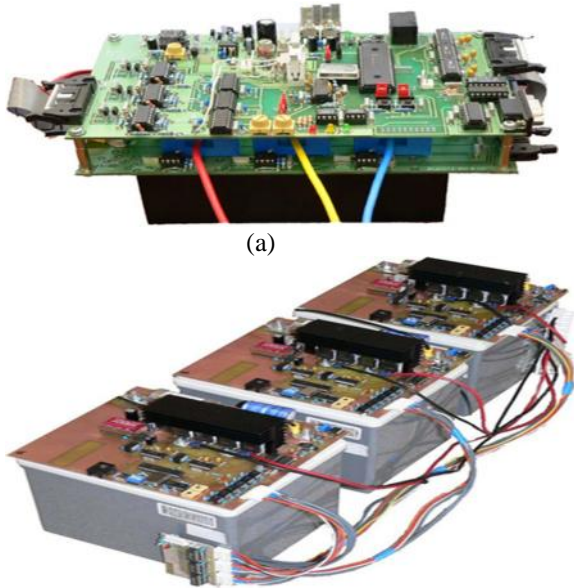
Prototype Hardware

To compare the performance of 2-level and multilevel converters, two prototypes have been constructed. These are shown in Figure 3; (a) shows the 2-level prototype and (b) the 7-level prototype, both being specified to drive the same 1.2 kW, brushless PM machine.

Embedded processors on each of the H-bridge cells produce the PWM signals and implement SoC estimation whilst receiving cell state input from the controller and returning SoC information. The controller calculates the states required to produce the demand and selects which cell produces the output based on the received SoC. Both prototypes use a PIC18F4431 series microcontroller as the embedded processor, with each H-bridge cell using a PIC18F2431 which communicates via an optically isolated SPI interface.

The 7-level prototype consists of three H-bridge cells, (A, B, C) and a phase controller, each H-bridge cell using a 12V 30Ah sealed lead acid battery. 7 voltage levels are chosen as it provides a significant reduction in current ripple and at least three battery levels are required to evaluate the battery management schemes. However, the construction of the system uses identical cells on a common interface bus providing a modular, readily expandable system with built-in redundancy.

The switching devices used in the 2-level converter are Philips SenseFETs BUK7909 MOSFETs, rated at 75V and 75A. Two MOSFETs are used in parallel for each switch and low side current sensing is implemented removing the need for external sensors. The MLC H-bridge cells use FQA170N06 60V, 150A MOSFETs. For comparison the same switching frequency of 20 kHz is used for both prototypes.



(a)

(b)

Figure 6: Prototype Hardware, (a) 2-level converter, (b) 7-level converter

V. Simulation And Results

The three phase five level diode clamped multilevel inverter fed BLDC motor speed is controlled by PI controller. Speed is given feedback to PI controller. It compares actual speed and reference speed to produce error signal that is input for PI controller. Back EMF is under process and multiplied with PI output. These are used to give reference signal for sinusoidal PWM. Diode Clamped Multilevel Inverter three phase AC output is connected to BLDC motor terminals. Five level diode clamped multi-level inverter for three phases have three legs. For each leg eight switches used (upper leg 4 and lower leg 4 switches). Across the switches freewheeling diodes are connected for protection purpose. Switching pulses are given from the Sinusoidal Pulse Width Modulation Technique.

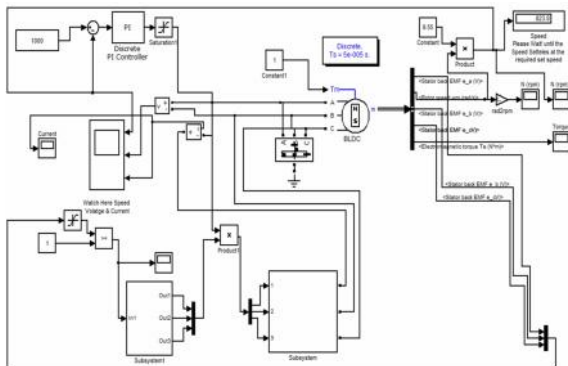


Fig 7. Simulation diagram for five level diode clamped multilevel inverter fed BLDC motor

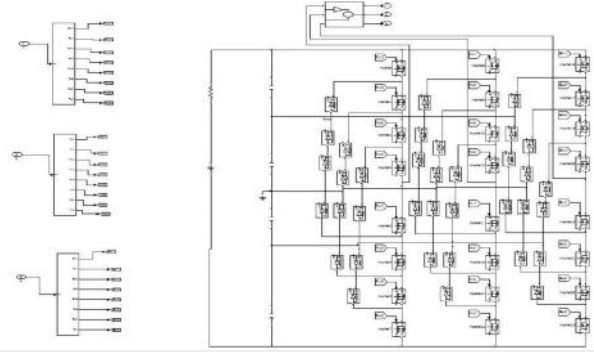


Fig 8. Simulation diagram for five level diode clamped multi-level inverter

Figure 8 show the simulation diagram of five level diode clamped multilevel inverter. Here subsystem represents the PWM generation circuit, using this circuit reference signal and four sine wave signals with different amplitude are compared. When the reference amplitude is greater than carrier amplitude the gate pulses are produced. Based on this gate pulses five level diode clamped multilevel inverter switches are made ON and OFF.

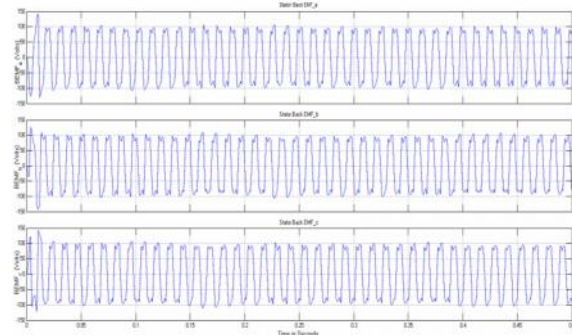


Fig 9. Stator Back EMF

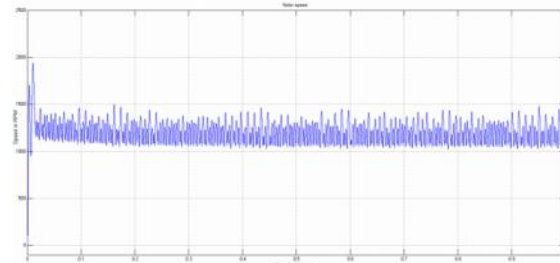


Fig 10. Output Speed

From the above Fig. 10 shows the output speed of three phase five level diode clamped multilevel inverter fed BLDC motor. Output speed can be controlled by PI controller (closed loop control). Speed can change by varying reference speed or set speed. Here the reference speed is 1200rpm and speed vary periodically due to steady state errors in PI controller.

VI. Torque Ripple Calculation

BLDC motor torque pulsations produce noise and vibration in the system. So minimization or elimination of noise and vibration is a considerable problem in BLDC Motor. Two techniques are mainly used to minimize the

Torque Pulsations. To improve motor design and motor control schemes. Fig. 7 shows the electromagnetic torque of BLDC motor. Torque ripple is defined as periodic increase and decrease in output torque. The formula for finding the torque ripple the percentage of the difference between the maximum torque (T_{max}) and the minimum torque (T_{min}) compared to the average torque (T_{avg}). Percentage Torque ripple can be calculated by the following formula,

$$\frac{(T_{max} - T_{min})}{T_{avg}} * 100$$

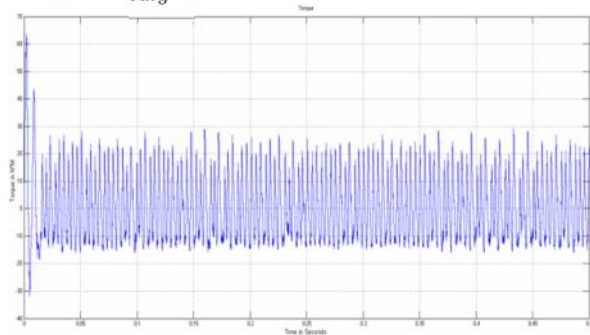


Fig 11. Electromagnetic Torque

Let us take the above said values from the Fig. 11 for one cycle. The maximum value of torque (T_{max}) is 24.4374, minimum value of the torque (T_{min}) is 15.8052 and the average value of this torque (T_{avg}) is 20.12. By substituting the above obtained values in equation (5) we get the torque ripple value is 42.90%. Still further reduction in torque ripple can be achieved by selecting optimum value of PI controller constants.

VII. Conclusion

Torque pulsations in BLDC motors brought about by the deviation from ideal conditions are either related to the design factors of the motor or to the power inverter supply, thereby resulting in non-ideal current waveforms. Undesirable torque pulsation in the BLDC motor drive causes speed oscillations and excitation of resonances in mechanical portions of the drive, leads the audible noise and visible vibration patterns in high precision machines. In this paper, a five level diode clamped multilevel inverter with PI controller is presented for BLDC. Torque ripples are due to in active phases. The torque ripples have been reduced using diode clamped multilevel inverter with the Sinusoidal Pulse width modulation technique. PI controller is used to control the Speed. The BLDC motor is results are analysed and the amount of torque ripple also calculated. From the simulated results it is evident that the torque ripples are reduced. The main advantage of this method is it uses sensor less technique for the three phases, so it reduces the sensor cost. This paper presents the concept of Cascade H-Bridge multi 5-level inverter connected to three phase stator winding of BLDCM with current control and speed control techniques to improve the performance of BLDCM and reduce the torque ripples and harmonics, calculate the total harmonic distortion. The design of the inverter

topology and phase shift pulse width modulating technique are carried out for five level cascade H bridge inverter fed BLDC motor drive and the simulation results are presented for the performance of the motor. It is also understood that when torque ripple reduces the THD also reduces and there by performance of the machine is improved.

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