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Development Of A Modified Svm Algorithm For Controlling The Rec Z-Source Npc Inverter

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Abstract:
The REC Z-source NPC inverter is accepted to come across applications in grid connected distributed generation (DG) systems based on renewable energy sources such as photovoltaic systems, wind turbines and fuel cell stacks. Two DG systems can be connected to the grid with only one REC Z-source NPC inverter thus plummeting the volume and cost while rising efficiency and facilitating control. The modulation of the REC Z-source NPC inverter was described using the carrier-based approach. However the space vector modulation (SVM) approach offers better harmonic performance compared with carrier-based pulse width modulation (PWM) strategy without zero-sequence voltage injection and can more expediently handle overall switching patterns and constraints and it is simple to implement.

Keywords: Buck–boost, neutral point clamped inverter, Z-source inverter, space vector modulation (SVM).

Introduction:

The Z-source concept can be applied to all dc-to-ac, ac to- dc, ac-to-ac and dc-to-dc power conversion whether two-level or multilevel. However multilevel converters offer many benefits for higher power applications. This paper presents the control of a Z-source neutral point clamped inverter using the space vector modulation technique. This gives a number of benefits both in terms of implementation and harmonic performance. The adopted approach enables the operation of the Z-source arrangement to be optimized and implemented digitally without introducing any extra commutations. In spite of its effectiveness in achieving voltage buck–boost conversion the Z-source NPC inverter proposed is expensive because it uses two Z-source networks, two isolated dc sources and requires a complex modulator for balancing the boosting of each Z-source network. The operational analysis and optimal control of the reduced element count (REC) Z-source NPC inverter was subsequently described.

Related Work:

Multilevel converters proffer many benefits for higher power applications which include an ability to synthesize voltage waveforms with lower harmonic content than two-level converters and operation at higher dc voltages using series connection of a basic switching cell of one type or another. Previous publications have shown the control of a Z-source neutral point clamped inverter using the carrier-based modulation technique.

Existing Method:

The three most common topologies are the cascaded inverter, the diode clamped inverter, and the capacitor clamped inverter. Among the three, the three level diode clamped also known as the neutral point clamped (NPC) inverter has become an established topology in medium voltage drives and is arguably the most popular certainly for three-level circuits.

Disadvantages:

The NPC inverter is constrained by its inability to produce an output line-to-line volt- age greater than the dc source voltage. For applications where the dc source is not always constant, such as a fuel cell, photovoltaic array and during voltage sags, etc., a dc/dc boost converter is often needed to boost the dc voltage to meet the required output voltage or to allow the nominal operating point to be favourably located. This increases the system complexity and is desirable to eliminate if possible.

Proposed Method:

The Z-source concept can be applied to all dc-to-ac, ac-to-dc, ac-to ac and dc-to-dc power conversion whether two-level or multilevel. The Z-source concept was extended to the NPC inverter where two additional Z-source networks were connected between two isolated dc sources and a traditional NPC inverter.

Advantages:

To overcome the cost and modulator complexity issues the design and control of an NPC inverter using a single Z-source network. The power quality of current injected to the grid is improved because of the three-level structure. It can also find use in adjustable speed drive systems in applications such as conveyor belts, fans, and water pumps.

System Architecture:

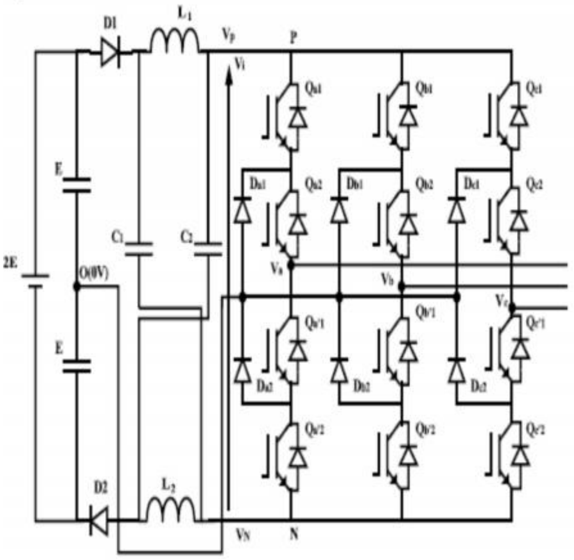

Fig.1. Topology of an REC Z-source NPC inverter.

The operation of each inverter phase leg of a traditional NPC inverter can be represented by three switching states P, O, and N. Switching state "P" denotes that the upper two switches in a phase leg are gated ON, "N" indicates that the lower two switches conduct, and "O" signifies that the inner two switches are gated ON. However, each phase leg of the Z-source NPC inverter has three extra switching states which resemble the "O" state of the traditional NPC inverter. These extra switching states occur when all the four switches in any phase leg are gated ON [full-shoot-through (FST)], or the three upper switches in any phase leg are gated ON [upper-shoot-through (UST)] or the three bottom switches in any phase leg are gated ON [lower shoot- through (LST)]. These shoot-through states are forbidden in the traditional NPC inverter because they would cause a short circuit of the dc-side capacitors. Again the Z-source network makes these shoot-through states allowable and provides the means for boost operation.

Z-Source Concept:

The only difference between the Z-source inverter and a traditional voltage source inverter (VSI) is the presence of a Z-source network comprising a split-inductor (*L*1 and *L*2) and two capacitors (*C*1 and *C*2). The unique feature of the two-level Z-source inverter is that the output ac voltage fundamental can be controlled to be any value between zero and infinity regardless of the dc source voltage. Thus, the Z-source inverter is a buck–boost inverter that has a very wide range of obtainable output voltage. Traditional VSIs cannot provide such features.

Switching States Of An Rec Z Source Npc Inverter:

State Type	ON Switches	ON Diodes	Vxo	Switching State
NST	Qx1,Qx2	D1,D2	$+V_i/2$	P
NST	Qx2,Qx'1	D1,D2,{Dx1 or Dx2}	0	0
NST	Qx'1,Qx'2	D1,D2	$-V_i/2$	N
FST	Qx1,Qx2,Qx'1,Qx'2	–	0	FST
UST	Qx1,Qx2,Qx'1	Dx2,D1	0	UST
LST	Qx2,Qx'1,Qx'2	Dx1,D2	0	LST

Table.1. Switching states of an REC Z-source NPC inverter

The REC Z-source NPC inverter is supplied with a split dc source. The middle point *O* is taken as a reference while controlling the switches of each phase leg according to the combinations presented in Table 1. Each output phase voltage $Vxo(x\_\{a, b, c\})$ has three possibilities: $Vi/2$, 0, and $-Vi/2$. When the REC Z-source NPC inverter is operated without any shoot-through states, then *Vi* is equivalent to 2E.

Circuit Analysis:

Two new switching states namely the UST and LST states were identified in addition to the FST state and the non shoot- through (NST) states (P, O, and N) that had been reported earlier. Although operation using the FST and NST states is possible (termed the FST operating mode) it is generally preferable to use the UST and LST states in place of the FST states (termed the ULST operating mode). The ULST operating mode is preferred because it produces an output voltage with enhanced waveform quality. The simplest FST operating mode requires all four switches in a phase leg to be turned ON.

Space Vector Diagram:

The reference vector *V*ref can be expressed as

$$V_{\text{ref}}(t) = \frac{2}{3}\left[V_{ao}(t)e^{j0} + V_{bo}(t)e^{j2\pi/3} + V_{co}(t)e^{j4\pi/3}\right]$$

The reference vector *V*ref is synthesized with three nearest space vectors, which are selected based on the triangle in which the reference vector is located at the sampling instant. If the reference vector is located in triangle 3, the nearest three vectors are *V*1, V7, and *V*13, respectively. Let the duty ratios of these vectors be denoted by *d*1, *d*2, and *d*3, respectively

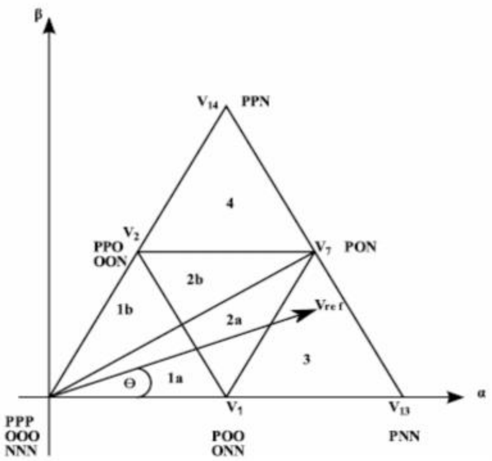

Fig.2. Space vector diagram of sector 1 for a three-level inverter.

Switching Sequence And Insertion Of Shoot-Through States:

In order to introduce shoot-through states, it is necessary to determine where the UST and LST states can be inserted, and on which phase, in order that the normalized volt–second area applied to the load is unchanged from the standard NPC case discussed above. In addition, it is desirable to ensure that no extra commutations are introduced. Theoretically, a shoot-through state can be introduced on any phase which is switched to the zero level (O) without affecting that phase voltage. However, the effect on the line-to-line voltages must also be taken into account. Note that when any phase has UST applied, the positive rail (P) is at the same potential as the dc mid-point (O). Similarly, during LST, the negative rail (N) is at the same potential as the dc mid-point (O). Consequently, it is only possible to use the UST state on a given phase when it is connected to O and the other two phases are connected either to O or N in order to get the correct line-to-line voltages. Similarly, an LST state can only be used when the other two phases are O or P.

Simulation Results:

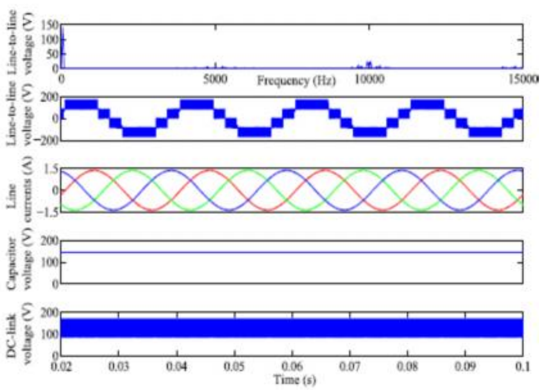

Fig.3. Simulated waveforms of REC Z-source inverter using ULST strategy.

Result shows the corresponding boosted inverter waveforms. The spectrum of the line-to-line voltage shows a peak fundamental value of 140 V compared to an expected value of 149 V. Also, the dc-link voltage has been boosted to 170 V, compared to an expected value of 184 V. It is also noted that the line currents are not distorted even when shoot-through states are intentionally inserted into the appropriate phase legs because of the presence of the Z-source network. The voltage across the Z-source capacitors is boosted to 145 V compared to an expected value of 152 V. In addition, the dc-link voltage seen by the NPC circuitry assumes two distinct levels of almost 170 and 85 V, respectively. From the simulation results, it is noted that there are slight errors between the expected and actual values.

Conclusion:

The presented concepts have been verified in simulation. Using carefully inserted UST and LST states to the traditional NPC inverter state sequence, the REC Z-Source NPC inverter functions with the correct volt–second average and voltage boosting capability regardless of the angular position of the reference vector. The insertion of the shoot through states was such that the number of device commutations was kept at a minimum of six per sampling period, similar to that needed by a traditional NPC inverter.

References:

[1] S. Busquets-Monge, J. Rocabert, P. Rodriguez, S. Alepuz, and J. Bordonau, “Multilevel diode-clamped converter for photovoltaic generators with independent voltage control of each solar array,” *IEEE Trans. Ind. Electron.*, vol. 55, no. 7, pp. 2713–2723, Jul. 2008.

[2] J. Zhao, Y. Han, X. He, C. Tan, J. Cheng, and R. Zhao, “Multilevel circuit topologies based on the switched-capacitor converter and diode-clamped converter,” *IEEE Trans. Power Electron.*, vol. 26, no. 8, pp. 2127–2136, Aug. 2011.

[3] J.-S. Hu, K.-Y. Chen, T.-Y. Shen, and C.-H. Tang, “Analytical solutions of multilevel space-vector PWMfor multiphase voltage source inverters,” *IEEE Trans. Power Electron.*, vol. 26, no. 5, pp. 1489–1502, May 2011.

[4] Z. Zhao, Y. Zhong, H. Gao, L. Yuan, and T. Lu, “Hybrid selective harmonic elimination PWM for common-mode voltage reduction in threelevel neutral-point-clamped inverters for variable speed induction drives,”*IEEE Trans. Power Electron.*, vol. 27, no. 3, pp. 1152–1158, Mar. 2012.

[5] P. Sun, C. Liu, J.-S. Lai, and C.-L. Chen, “Cascade dual buck inverter with phase-shift control,” *IEEE Trans. Power Electron.*, vol. 27, no. 4, pp. 2067–2077, Apr. 2012.[6] J. Ebrahimi, E. Babaei, andG.Gharehpetian, “Anewtopology of

cascaded multilevel converterswith reduced number of components for high-voltage applications," *IEEE Trans. Power Electron.*, vol. 26, no. 11, pp. 3109– 3118, Nov. 2011.

[7] C. Govindaraju and K. Baskaran, "Efficient sequential switching hybridmodulation techniques for cascaded multilevel inverters," *IEEE Trans. Power Electron.*, vol. 26, no. 6, pp. 1639–1648, Jun. 2011.

[8] J. Shen, S. Schroeder, R. Roesner, and S. El-Barbari, "A comprehensive study of neutral-point self-balancing effect in neutral-point-clamped threelevel inverters," *IEEE Trans. Power Electron.*, vol. 26, no. 11, pp. 3084– 3095, Nov. 2011.

[9] J. Li, J. Liu, D. Boroyevich, P. Mattavelli, and Y. Xue, "Three-level active neutral-point-clamped zero-current-transition converter for sustainable energy systems," *IEEE Trans. Power Electron.*, vol. 26, no. 12, pp. 3680–3693, Dec. 2011.

[10] H. Xiao and S. Xie, "Transformerless split-inductor neutral point clamped three-level PV grid-connected inverter," *IEEE Trans. Power Electron.*, vol. 27, no. 4, pp. 1799–1808, Apr. 2012.

[11] J. Pou, J. Zaragoza, S. Ceballos, M. Saeedifard, and D. Boroyevich, "A carrier-based PWM strategy with zero-sequence voltage injection for a three-level neutral-point-clamped converter," *IEEE Trans. Power Electron.*, vol. 27, no. 2, pp. 642–651, Feb. 2012.

[12] S. Jayasinghe, D. Vilathgamuwa, and U. Madawala, "Diode-clamped three-level inverter-based battery/supercapacitor direct integration scheme for renewable energy systems," *IEEE Trans. Power Electron.*, vol. 26, no. 12, pp. 3720–3729, Dec. 2011.

[13] T. Meynard and H. Foch, "Multi-level conversion: High voltage choppers and voltage-source inverters," in *Proc. Conf. Rec. 23rd Annu. IEEE Power Electron. Special. Conf.*, Jul. 1992, vol. 1, pp. 397–403.

[14] S. Thielemans, A. Ruderman, B. Reznikov, and J. Melkebeek, "Improved natural balancing with modified phase-shifted PWM for single-leg fivelevel flying-capacitor converters," *IEEE Trans. Power Electron.*, vol. 27, no. 4, pp. 1658–1667, Apr. 2012.

[15] B. McGrath and D. Holmes, "Enhanced voltage balancing of a flying capacitor multilevel converter using phase disposition (PD) modulation," *IEEE Trans. Power Electron.*, vol. 26, no. 7, pp. 1933–1942, Jul. 2011.