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A High Speed Vedic Multiplier Using Different Compressors

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Abstract
A digital clock rate multiplier, divisor using variable point math which generates the output clock with almost zero occurrence error has been presented. The circuit has an uncontrolled multiplication and division factor range and short lock time. A short power method has been incorporated to ensure that the overall power consumption of the circuit is low. The circuit has been premeditated in TSMC 65nm CMOS process for an input allusion time of 0.01ns and has been tested with indiscriminate multiplication factor values, we present a novel architecture to perform high speed multiplication using ancient Vedic math's techniques. A new high speed approach utilizing 4:2 compressors and novel 7:2 compressors for addition has also been incorporated in the same and has been discovered. Upon evaluation, the compressor based multiplier introduced in this paper, is nearly two times faster than the popular methods of multiplication. With regards to area, a 1% diminution is seen. The design and tests were carried out on a Xilinx Spartan 3e series of FPGA and the timing and area of the design, on the similar have been calculated.

Keywords
4:2 Compressor, 7:2 Compressor, Booth's Multiplier, High Speed Multiplier, Modified Booth's Multiplier, Urdhwa Tiryakbhyam Sutra, Vedic Mathematics

I. Introduction

Many transform considered the doyen of this discipline, in his formative book algorithms like Fast Fourier transforms (FFTs), DFT etc. make Vedic Math, wrote about this distinct use of sutras[J I).use of multipliers [2], [3], [4]. With advances in knowledge, Vedic Mathematics" was the name given by him. He was one among many researchers have tried to design multipliers which offer individual who collected lost formulae from the writings of high speed, low power consumption, constancy of layout and "Atharwa Vedas" and wrote them in the form of Sixteen Sutras hence less area or even combination of them in multiplier and 13 sub-sutras. Vedic Mathematics is based on sixteen in recent times, high-speed multipliers [5] play a crucial sutras dealing with mathematics related to arithmetic's, algebra, role while designing any architecture and researchers are still and geometry. These methods and ideas can be directly applied working on many factors to increase the speed of operation of two trigonometry, plain and spherical geometry, conics, calculus these basic elements. Algorithms for designing high-speed and functional mathematics of different kinds. The Vedic methods multipliers have been altered and advanced for better are direct, and truly amazing in their efficiency [6]. The increased complexity of various simplicity. Research is being carried out in many parts, functions, demands not only faster multiplier chips but also including the effects on children who learn Vedic math's and the smarter and efficient multiplying algorithms that can be development of new, powerful but easy applications executed in the chips. It is up to the necessity of the hour and Vedic sutras in geometry, calculus, computing etc. But the real the application on to which the multiplier is implemented and beauty and efficiency of Vedic mathematics cannot be fully what tradeoffs need to be reflected. Generally, the efficiency valued without actually practicing the system. The speed of a processor highly depends on its multiplier's performance. By these algorithms, the multiplication process, involves several transitional operations before arriving at the final answer.

II. Vedic Math's - Urdhwa Tiryakbhyam Sutra

As mentioned earlier, Vedic Mathematics can be divided into 16 different sutras to perform mathematical calculations. Among these the Urdhwa Tiryakbhyam Sutra is one of the most highly preferred algorithms for performing multiplication. The algorithm is competent enough to be employed for the multiplication of integers as well as binary numbers. The term "Urdhwa Tiryakbhyam" originated from 2 Sanskrit words Urdhwa and Tiryakbhyam which mean "vertically" and "crosswise" respectively. The main advantage of utilizing this algorithm in comparison with the existing multiplication techniques, is the fact that it utilizes only logical "AND" operations, half adders and full adders to complete the multiplication operation. Also, the partial products required for multiplication are generated in parallel and apriority to the actual addition thus saving a lot of processing time.

Let us consider two 8 bit numbers A7-A0 and B7-B0, where 0 to 7 represent bits from the Least Significant Bit (LSB) to the Most Significant Bit (MSB). P0 to P15 represent each bit of the final computed product. It can be seen from equation (1) to (15), that P0 to P15 are calculated by adding partial products, which are calculated

previously using the logical AND operation. The individual bits obtained from equations (1) to (15), in turn when concatenated produce the final product of multiplication which is depicted in (16).The carry bits generated during the calculation of the individual bits of the final product are represented from C1 to C30. The carry bits generated in (14) and (15) are ignored since they are superfluous.

P0 =A0 * B0 (1)

C1P1 = (A1 * B0) + (A0 * B1) (2)

C3C2P2 = (A2 * B0) + (A0 * B2) + (A1 * B1) + C1 (3)

C5C4P3 = (A3 * B0) + (A2 * B1) + (A1 * B2) + (A0 * B3) +C2 (4)

C7C6P4 = (A4 * B0) + (A3 * B1) + (A2 * B2) + (A1 * B3) + (A0 * B4) + C3 + C4 (5)

C10C9C8P5 = (A5 * B0) + (A4 * B1) + (A3 * B2) + (A2 * B3) + (A1 * B4) + (A0 * B5) + C5 + C6 (6)

C13C12C11P6 = (A6 * B0) + (A5 * B1) + (A4 * B2) + (A3 * B3) + (A2 * B4) + (A1 * B5) + (A0 * B6) +C7 + C8 (7)

C16C15C14P7 = (A7 * B0) + (A6 * B1) + (A5 * B2) + (A4 * B3) + (A2 * B5) + (A1 * B6) + (A0 * B7) +C9 + C11 (8)

C19C18C17P8 = (A7 * B1) + (A6 * B2) + (A5 * B3) + (A4 * B4) + (A3 * B5) + (A2 * B6) + (A1 * B7) + C10 +C12 + C14 (9)

C22C21C20P9 = (A7 * B2) + (A6 * B3) + (A5 * B4) + (A4 * B5) + (A3 * B6) + (A2 * B7) + C13 +C15 +C17 (10)

C25C24C23P10 = (A7 * B3) + (A6 * B4) + (A5 * B5) + (A4 * B6) + (A3 * B7) + C16 + C18 + C20 (11)

C27C26P11 = (A7 * B4) + (A6 * B5) + (A5 * B6) + (A4 * B7) + C19 +C21 + C23 (12)

C29C28P12 = (A7 * B5) + (A5 * B6) + (A5 * B7) + C22 + C24 +C26 (13)

C30P13= (A7 * B6) + (A6 * B7) + C25 + C27 + C28 (14)

P14 = (A7 * B7) + C29 + C30 (15)

P15= (A7 * B7) (16)

Fig.1 graphically illustrates the step by step method of multiplying two 8 bit numbers using the Urdhwa Tiryakbhyam Sutra. The black circles indicate the bits of the multiplier and multiplicand, and the two-way arrows indicate the bits to be multiplied in order to arrive at the individual bits of the final product.

The hardware architecture of the 8x8 Urdhwa multiplier has been designed and shown in fig. 2

As mentioned earlier, the partial products obtained are added with the help of full adders and half adders. It can be seen, from equation (1) to (16) that in few equations there is a necessity of adding more than 3 bits at a time. This leads to additional hardware and additional stages, since the full adder is capable of adding only 3 bits at a time. In the next section two different types of compressor architectures are explored which assist in adding more than 3 bits at a time, with reduced architecture and increased efficiency in terms of speed.

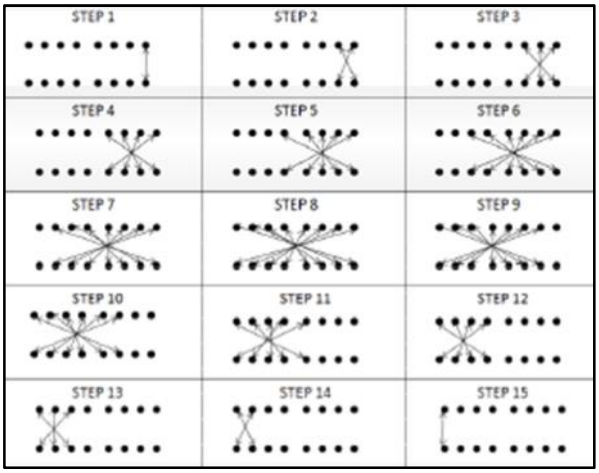

Fig. 1: Pictorial Illustration of Urdhwa Tiryakbhyam Sutra for Multiplication of 2 Eight Bit Numbers

III. Compressor Adder

A compressor adder is a logical circuit which is used to improve the computational speed of the addition of 4 or more bits at a time. Compressors can efficiently replace the combination of several half adders and full adders, thereby enabling high speed performance of the processor which incorporates the same. The compressor adder used in this paper is a 4:2 compressor adder. A lot of research in the past has been carried out on the same. This has been elaborated below. A comparison of the 4:2 compressor with an equivalent circuit, using full adders and half adders has also been given below.

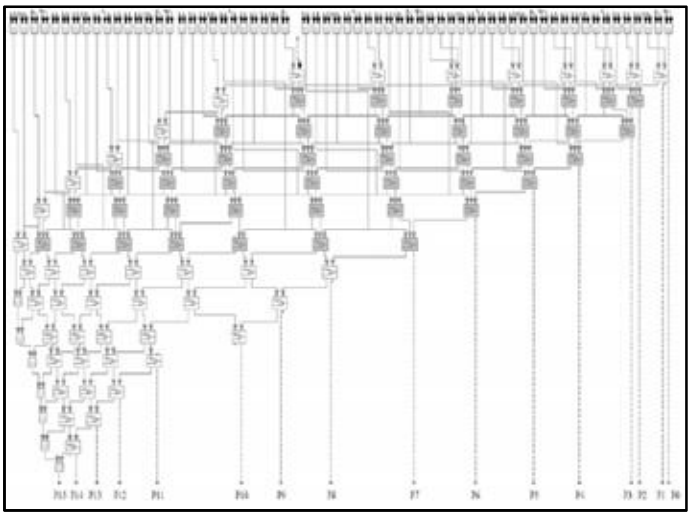

Fig 2: Hardware architecture of 8*8 Urdhwa multiplier

A. 4:2 Compressor Adder

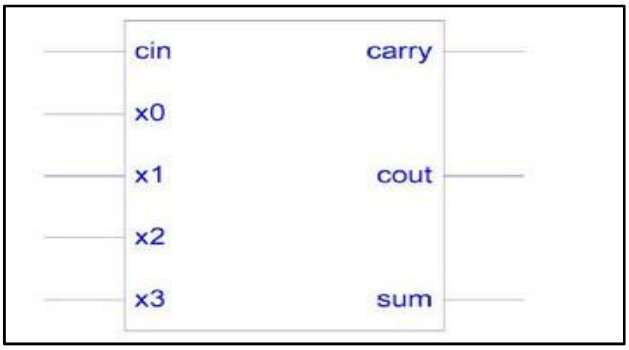

Fig. 3: Black Box of a 4:2 Compressor Adder

A 4:2 compressor as shown in fig.3. Is capable of adding 4 bits and one carry, in turn producing a 3 bit output. The internal architecture of the same has been show in fig. 4. It can be clearly seen, the critical path is smaller in comparison with an equivalent circuit to add 5 bits using full adders and half adders. For the sake of comparison, the equivalent circuit to add 5 bits has also been shown in fig. 5.

Let us consider the propagation delay of a gate to be tp. It is well known that a full adder has a total propagation delay of 2tp and a half adder has a propagation delay of tp. Considering this, the total propagation delay of a 4:2 adder using full adders and half adders can be calculated as 5tp and can be seen in fig. 5. On the other hand, it can be seen from fig. 4. That the propagation delay of a 4:2 compressor remains only 3tp. Therefore, a 66.6% increase in speed can be recorded in comparison with an equivalent circuit made of full and half adders, proving to be a highly efficient architecture for addition.

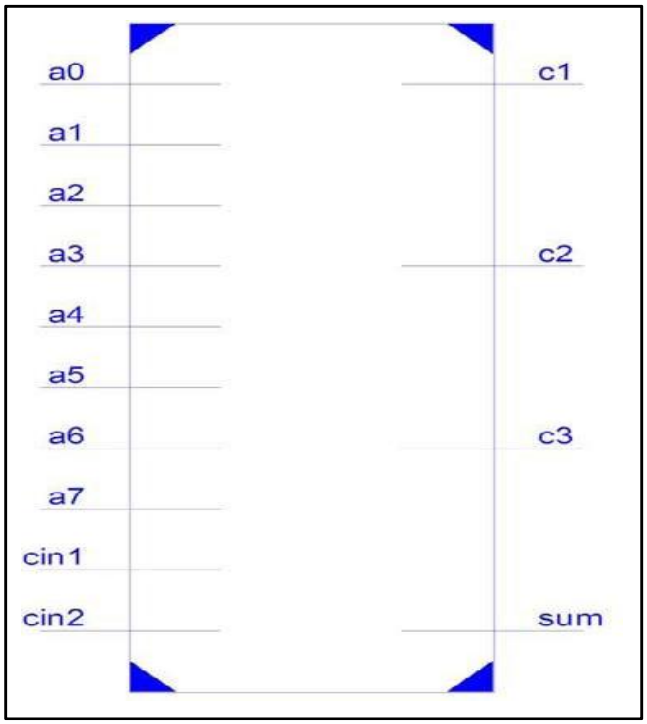

Fig. 4: Gate Level Diagram of 4:2 Compressor

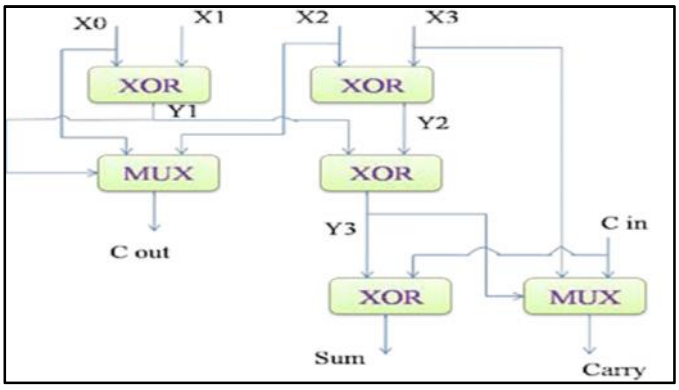

Fig. 5: 4:2 Compressor Using Full Adders and Half Adders

In order to add more than 5 bits at a time, yet another compressor architecture, the 7:2 compressor adder could be used and this is explained in detail below.

B. 7:2 Compressor Adder

Similar to its 4:2 compressor counterpart, the 7:2 compressor as shown in it. 6., is capable of adding 7 bits of input and 2 carry's from the previous stages, at a time. In our implementation, we have designed a novel 7:2 compressor utilizing two 4:2 compressors, two full adders and one half adder. The architecture for the same

has been shown in fig. 7.

As mentioned earlier, since the 4:2 compressor shows a significant increase in speed by around 66.6%, utilizing the same in this architecture would improve the efficiency as opposed to a conventional approach of adding nine bits at a time using only full adders and half adders. This leads to a great improvisation in speed of the processor. Through experimentation on a Xilinx Spartan-3e FPGA, it was found that the novel 7:2 compressor adder architecture introduced here is 1.05 times faster than a conventional approach. This result justifies the need of utilizing this compressor in our design.

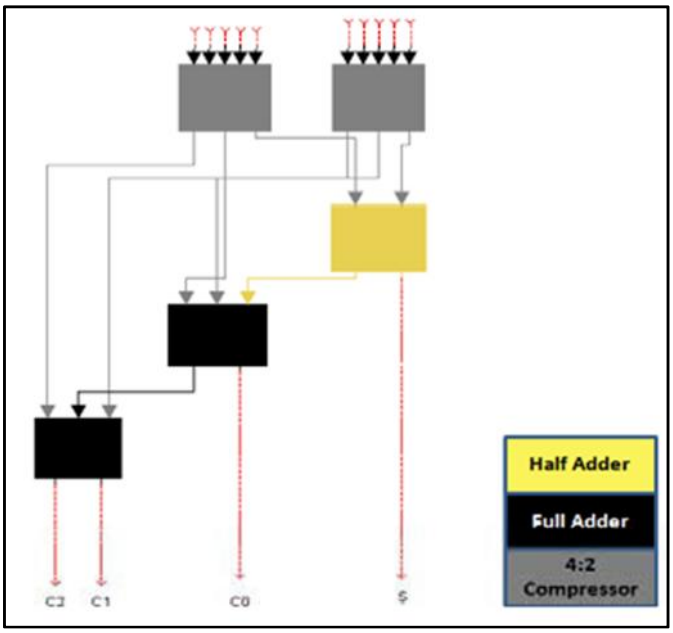

Fig. 6: Black Box Representation of a 7:2 Compressor Adder

The next section discusses a novel approach to combine the efficiency of the compressor architectures introduced above with the existing Vedic mathematics approach for multiplication.

IV. Compressor Based Urdhwa Tiryakbhyam Multiplier As mentioned in Section II, the multiplier based on Urdhwa method of multiplication requires several full adders and half adders to add the necessary partial products. This in turn leads to a large propagation delay due to the reasons explained in the previous section. As part of our novel approach, we combined the compressor architectures explained earlier and utilized the same in the Urdhwa based architecture which was formerly shown in fig.

2. The architecture for the same has been shown below in fig. 8. It can be clearly seen from fig. 8 that the compressor based Urdhwa multiplier requires only 12 parallel stages as opposed to 15 which was in the case of the conventional Urdhwa Tiryakbhyam multiplier. This is a major improvement with respect to high speed multiplier design. Also, it can be seen that, many of the stages have now been reduced to a mere logical XOR operation, with an initiative to reduce area.

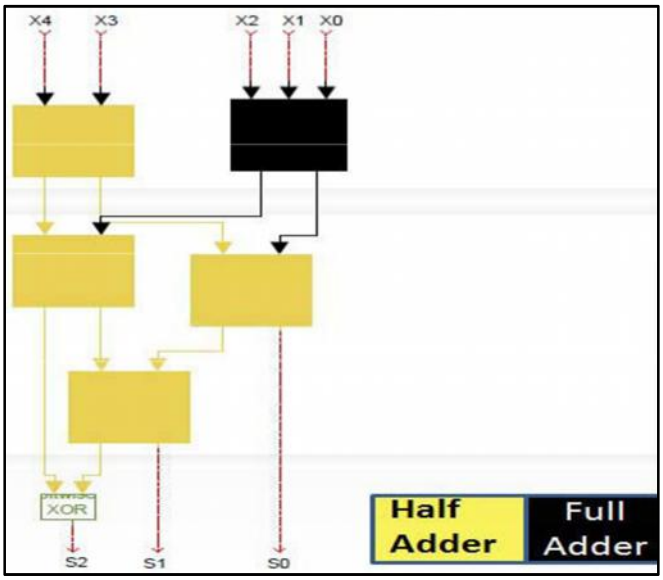

Fig. 7: 7:2 Compressor Using 4:2 Compressor Adder

Fig. 8: Hardware Architecture of Compressor Based Urdhwa Multiplier

An analysis on the area occupied by the new design and also the improvement in speed in comparison with other popular methods of multiplication has been presented in the next section.

V. Results

In order to perform a comparison, various popular multipliers

– Urdhwa multiplier and also the compressor based Urdhwa multiplier were implemented on a Xilinx Spartan 3e – XC3S500E FPGA using VHDL as the RTL language with the help of Xilinx Project Navigator 14.2. The codes were synthesized.
Unoptimized speed and area parameters were compared. The Spartan 3e FPGAused for the experiments has a speed grade of -5 and package CP132. The results have been tabulated in Table 1.

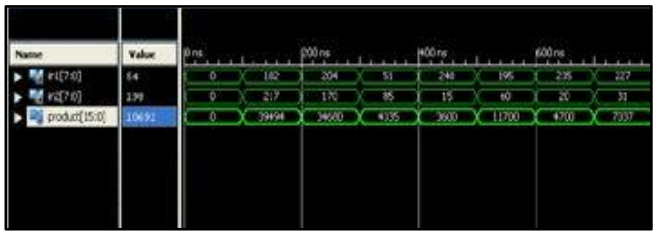

Fig. 9: Compressor Based Vedic Multiplier Wave Forms

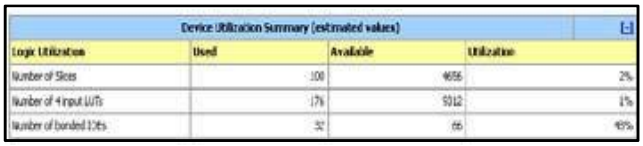

Fig. 10: Compressor Based Vedic Multiplier Synthesis Report

Table 1. Comparison of Area Occupied and Speed of Various Multiplier Architectures

Algorithm Used	LUTs	Total LU	Percentage of area	Time
Booth	56	9312	0.6	30.548
Modified Booth	215	9312	2.3	22.752
Urdhwa Tiryakb	190	9312	2	16.263
Compressor Based Urdhwa	176	9312	1	15.52

It can be clearly noted from Table I., that in terms of speed, the compressor based Vedic math's multiplier performs exceptionally well and is almost 1.12 times faster than the existing Vedic math's based multiplier. It can also be seen that in comparison with the booth and modified booth multipliers, the new architecture is around 2.112 times and 1.509 times faster respectively with regards to speed.
Another interesting thing to note is the area occupied. Since, the 4:2 compressor has reduced number of gates as compared to a full/ half adder based circuit, the area has also reduced equivalently. It can be seen that the compressor based multiplier has occupied an area 1% lesser than the Vedic math's and a 3% reduction with respect to the modified booth methodology is also seen. Even though the compressor based architecture occupies area more than that of the booths method, since speed is our major concern, this fact can be ignored.

VI. Conclusion

In this paper, we have proposed a novel high speed architecture for multiplication of two 8 bit numbers, combining the advantages of compressor based adders and also the ancient Vedic math's methodology. A new 7:2 compressor architecture, based on 4:2 compressor architecture was also discussed. Upon comparison of the area occupied by the multiplier and also its speed, with two other popular multipliers, we can conclude that the compressor based Vedic math's multiplier proves to be a better option over conventional multipliers used in several expeditious and complex VLSI circuits. As a future work, the multiplier's performance could be tested within an ALU and also compared with several other existing multipliers.

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