



## On-Chip AHB Bus Trace Analyzer for Real Time Tracing With Lossless Data Compression

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### ABSTRACT

The advanced micro controller bus Architecture (AMBA) is widely used as the on-chip bus in System-on-Chip(SoC) designs. The important aspect of a SoC is not only which components or blocks it houses, but also how they are interconnected. AMBA is a solution for the blocks to interface with each other. The objective of the AMBA specification is to be technology independent, minimize silicon infrastructure while supporting high performance and low power on-chip communication. The biggest challenge in SoC design is in validating and testing the system.

The Advanced High-performance Bus (AHB) is a part of the Advanced Microcontroller Bus Architecture (AMBA). Performance can be improved at high-frequency operation. Performance is independent of the mark-space ratio of the clock. No special considerations are required for automatic test insertion. Our aim in this project is to design the AHB- protocol with bus tracer. For real-time tracing, we should reduce the trace size as much as possible without reducing the original data.

The experimental results show that trace compression ratio reduced by 96.32%. Finally this approach was designed successfully along with MODEL SIM and synthesis using Xilinx ISE. The SoC can be verified in field-programmable gate array.

**Keywords:** AMBA, AHB Bus Tracer, Real Time Compression, multi-resolution, signal tracing.

### 1. INTRODUCTION

The Advanced Microcontroller Bus Architecture (AMBA) specification defines an on-chip communication standard for designing high-performance embedded microcontrollers. The AHB acts as the high-performance system backbone bus. AHB supports the efficient connection of processors, on-chip memories and off-chip external memory interfaces with low-power peripheral macrocell functions. AHB is also specified to ensure ease of use in an efficient design flow using synthesis and automated test techniques.

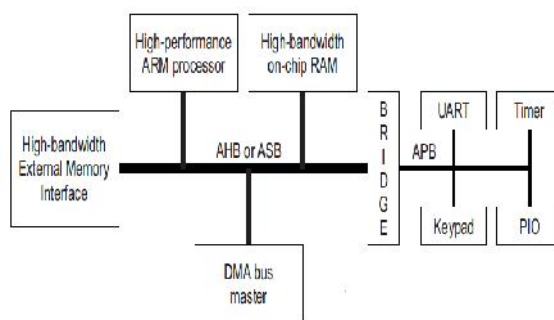


Fig 1. A Typical AMBA AHB based system

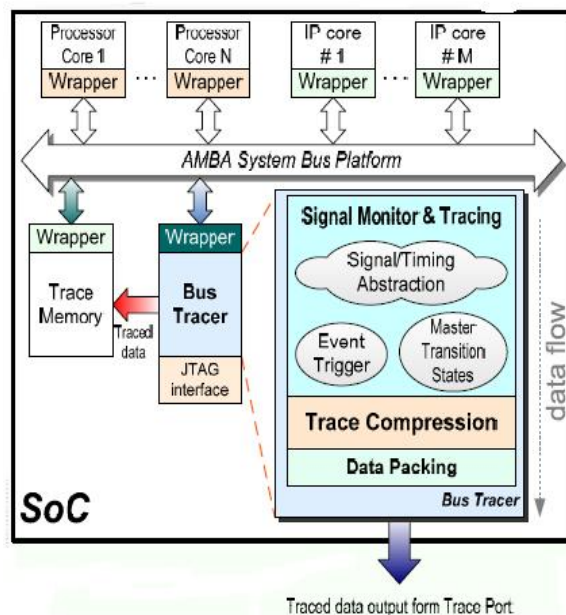
An AMBA AHB design may contain one or more bus masters, typically a system would contain at least the processor and test interface. However, it would also be common for a *Direct Memory Access* (DMA) or *Digital Signal Processor* (DSP) to be included as bus masters.

### 2. RELATEDWORK

The spirit of a hardware tracer is how to reduce the data using Compression mechanism. There are hardware approaches to compress the trace, which can be divided in lossy and lossless categories. Some appropriate compressing methods have been available for different types and parts of bus signals. Branch/target filtering is one common technique for program address compression. This approach has been used in some commercial processors, such as TriCore and ARM's Embedded Trace Macrocell. The hardware overhead of these works is small since the filtering mechanism is simple to implement in hardware. However, the effectiveness of these techniques is mainly limited by the average basic block size, which is roughly around four or five instructions per basic block, as reported in and for data address and value tracing, the most popular method is used the differential approach based on subtraction. Some researches have shown that using the differential method can reduce the data address and data values traces by about 40 percent and 14 percent respectively. Besides the address and data bus, there are several control signals on system bus that need to be traced. Some FPGA boards have built-in signal trace tools, such as the Altera Signal Tap and Xilinx Chip-Scope. FS2 AMBA Navigator supports bus clock mode and bus transfer mode to trace bus signals on every clock and bus transfer respectively. Trace buffer stores bus cycles or bus transfers based on local internal memory size. Although these approaches support multiple trace modes such as tracing at cycle by-cycle or at signal transaction, only one mode can use during a tracing process. This paper presents the multi-resolution approach that can use different trace modes during a bus signal tracing process.

### 3. AMBA BUS TRACER ARCHITECTURE

This section presents the architecture of our bus tracer. Shown in Fig.1 is the bus tracer overview. It mainly contains four parts 1)Event Generation Module 2)Abstraction Module 3)Compression Modules and 4)Packing Module. The Event Generation Module controls the start/stop time, the trace mode, and the trace depth of traces. The signal Abstraction module traces the corresponding AHB signals at proper time according to user configuration. The trace compression module compresses the trace data in accordance with signal characteristics. Finally, in the data packing module, the trace data is arranged compactly for output to the internal on-chip trace memory or external off-chip storage.



**Fig.2. Multiresolution Bus Tracer Block Diagram**

The transaction-level debugging provides software and hardware designers a common abstraction level to diagnose bugs. The abstraction level is in two dimensions timing abstraction and signal abstraction. The timing dimension has two abstraction levels which are the cycle level and transaction. level. The cycle level captures the signals at every cycle. The transaction level records the signals only when their value changes.

The signal dimension involves grouping of AHB bus signals into four categories: program address, data address/value, access control signals (ACS), and protocol control signals (PCS). Then, we define three abstraction levels for those signals. The master state level further abstracts the bus state level by only recording the transfer activities of bus masters and ignoring the handshaking activities within transactions. This level also ignores the signals when the bus state is IDLE, WAIT, and BUSY. The BSM is designed based on the AMBA AHB 2.0 protocol to represent the key bus handshaking activities within a transaction.

*1. Event Generation Module:* The Event Generation Module decides the beginning and ending of a trace and its trace mode. Depending on the combinations of address data and trace depth AHB decides to change the event depending upon its trace granularity and direction. The AHB checks all the events based on AHB protocol checker



levels pipeling stages has been indicated.Using pipeling stage it improves overall capability of the systems

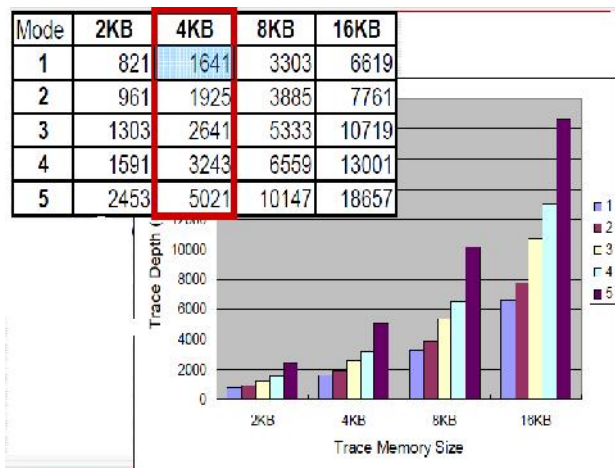


Fig.4. Trace Memory Vs Trace size

When the on chip trace memory is full, it sends an interrupt to the microprocessor then this processor reads the data from the trace memory and transfers the trace data to off-chip storage through AMBA.

	Original trace size (88bits/cycle)	Compression Ratio After Signal/Timing Abstraction and Trace Reduction				
		@ mode 1	@ mode 2	@ mode 3	@ mode 4	@ mode 5
Perpetual Calendar	880000	83.71%	83.79%	90.05%	94.67%	96.99%
Fib. Sequence	880000	78.51%	80.05%	87.91%	90.45%	94.73%
G.C.D.	880000	83.22%	83.45%	89.14%	92.76%	95.68%
Towers of Hanoi	880000	78.64%	80.61%	85.99%	88.58%	92.56%
Knight Problem	880000	83.96%	84.33%	96.39%	97.16%	98.32%
Quick Sort	880000	78.27%	79.99%	99.64%	99.71%	99.80%
Geometric mean	-	81.01%	82.02%	91.39%	93.81%	96.32%

4) *Packing Module*: The Packing Module is the last phase. It receives the compressed data from the compression module, processes them, and writes them to the trace memory.

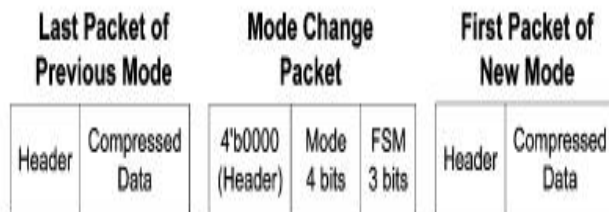


Fig.5.Concatenation of mode-change packet for abstraction mode switch  
4. AHB Protocol checker (HP checker)

Checker is an external module from where we can trace data other than AHB bus.

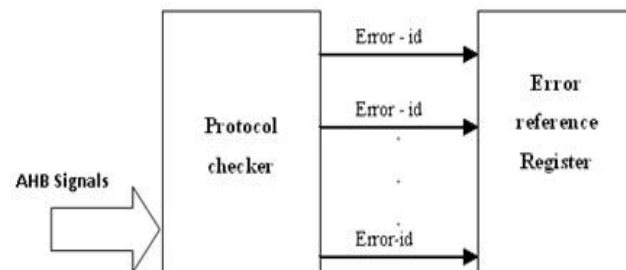


Fig. 5: Protocol Checker

AHB Protocol Checker (HP Checker) architecture, contains two main function blocks: Protocol Checker, ERROR Reference.

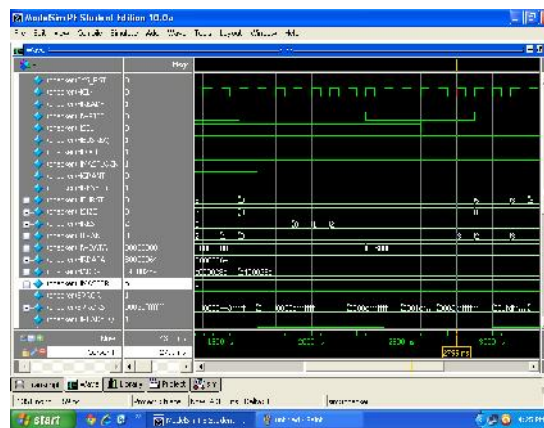
Protocol Checker is the main core of HP Checker, the inputs are all AHB bus signals, and the outputs are ERROR signals and corresponding master and slave IDs. Every rule has its own corresponded bit because every cycle maybe occur more than one error.

HP Checker is a rule-based protocol checker, thus how to establish a set of well-defined rules is very important.

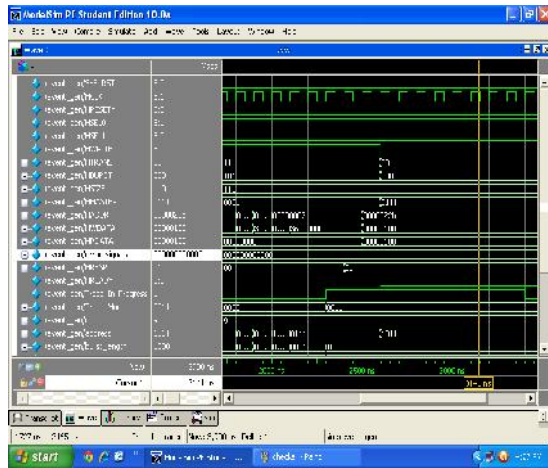
5. EXPERIMENTAL RESULTS

By simulation and synthesis the following results are obtained for each cycle at different abstraction levels. Here Modelsim tool is used in order to simulate the design and Xilinx tool for Synthesis process and the netlist generation.

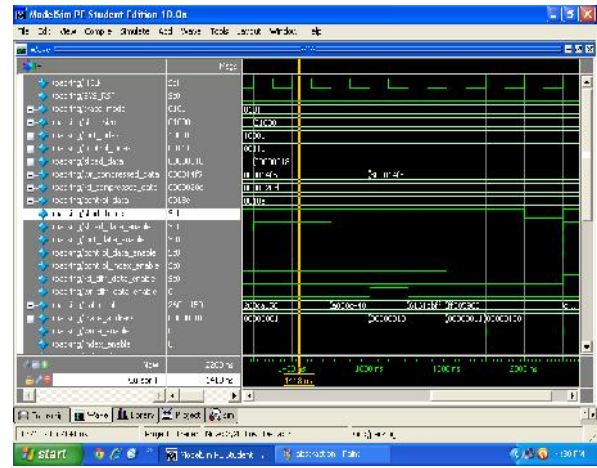
Checker Result:-



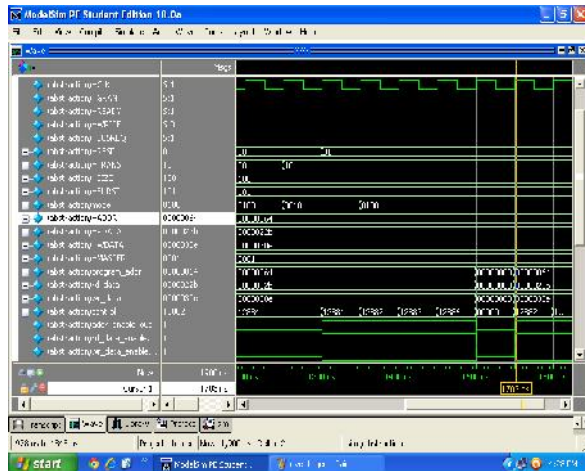
**Event Generator Result:-**



**Packing Result:-**

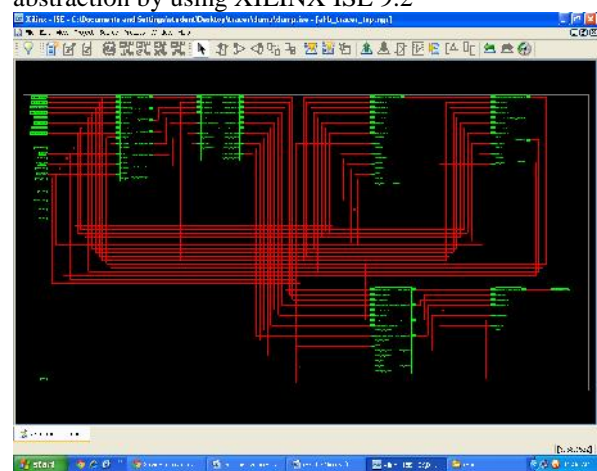


**Abstraction Result:-**

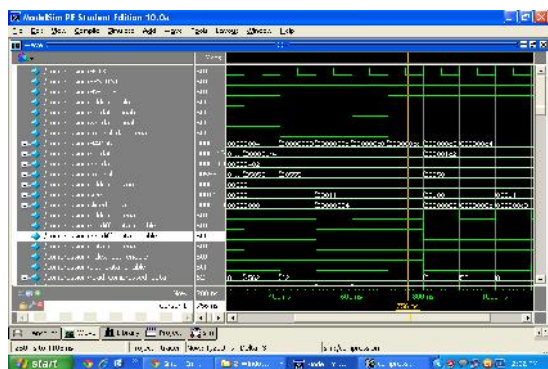


**Synthesis Result:-**

We synthesized this code by using XILINX ISE 9.2 verification, and implementation of digital logic chips at the Register transfer level (RTL) level of abstraction by using XILINX ISE 9.2



**Compression Result:-**



**DESIGN SUMMARY RESULT:-**

Device Utilization Summary			
Logic Utilization	Used	Available	Utilization
Number of Slices	8	330	2%
Number of Input LUTs	40	330	12%
<b>Logic Distribution</b>			
Number of occupied Slices	21	330	6%
Number of Slices occupied by dedicated logic	21	21	100%
Number of Slices occupied by unoccupied logic	0	21	0%
<b>Total Number of Input LUTs</b>	<b>40</b>	<b>330</b>	<b>12%</b>
Number of bonded I/Os	43	66	65%
Number of I/Os	1	2	50%
<b>Total equivalent gate count for design</b>	<b>35</b>		
Number of Configurable Logic Cells	232		

### Timing Summary:-

Minimum period: 5.654ns (Maximum Frequency:  
176.864MHz)

Minimum input arrival time before clock: 7.141ns

Maximum output required time after clock: 6.978ns

Maximum combinational path delay: 8.227ns

### CONCLUSION

AHB bus is capable of achieving high performance with a maximum frequency of 176.864MHz. The bus traces with 5 modes of resolution and the design is verified for all cases of 5 modes. With the aforementioned features, SYS-HMRBT supports a diverse range of design/debugging/ monitoring activities, including module development, chip integration, hardware/software integration and debugging, system behavior monitoring, system performance/power analysis and optimization, etc. The users are allowed to tradeoff between trace granularity and trace depth in order to make the most use of the on-chip trace memory or I/O pins. The reason is that this paper optimizes the pingpong architecture by sharing most of the data path.

### FUTURE SCOPE

In the future, we would extend this work to more advanced buses/connects such as AXI or OCP. In addition, with its real time abstraction capability, we would like to explore the possibility of bridging our bus tracer with ESL design methodology for advanced hardware/software procure development/debugging/ monitoring/analysis.

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